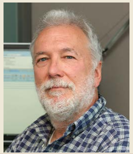
James R. Goodman
PhD University of California, Berkeley



USING CACHE MEMORY TO REDUCE PROCESSOR-MEMORY TRAFFIC

James R. Goodman
Department of Computer Sciences
University of Wisconsin-Madison
Madison, WI 53706

Honesty Young
Advised by James R. Goodman
Evaluation of a decoupled computer architecture and the design of a vector extension
First employment at IBM

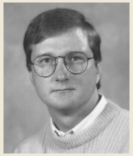
Gurindar S. Sohi
PhD University of Illinois at Urbana-Champaign

James E. Smith
PhD University of Illinois at Urbana-Champaign

Shlomo Weiss
Advised by James E. Smith
Very high performance scalar processing
First employment at University of Maryland

Wei-Chung Hsu
Advised by James R. Goodman
Register allocation and code scheduling for load/store architectures
First employment at Cray

Mark D. Hill
PhD University of California, Berkeley



Steve Kunkel
Advised by James E. Smith
Pipelined processing of fine-grain parallelism
First employment at IBM

Men-Chow Chiang
Advised by Gurindar S. Sohi
Memory System Design for Bus Based Multiprocessors
First employment at IBM

Instruction Issue Logic for High-Performance, Interruptible, Multiple Functional Unit, Pipelined Computers

David A. Wood
PhD University of California, Berkeley

Weak Ordering - A New Definition†
Sarita V. Adve
Mark D. Hill
Computer Sciences Department
University of Wisconsin
Madison, Wisconsin 53706

The Wisconsin Wind Tunnel: Virtual Prototyping of Parallel Computers*
Steven K. Reinhardt, Mark D. Hill, James R. Larus, Alvin R. Lebeck, James C. Lewis, and David A. Wood
Computer Sciences Department
University of Wisconsin–Madison
1210 West Dayton Street
Madison, WI 53706 USA
wwt@cs.wisc.edu

Mark Friedman
Advised by Gurindar S. Sohi
An Architectural Characterization of Prolog Execution
First employment at Trinity University

Steve Scott
Advised by James R. Goodman
Toward the design of large-scale, shared-memory multiprocessors
First employment at Cray Research

Manoj
Advised by Gurindar S. S
The Multiscalar Architect
First employment at Clem
University

1985

1990

Jian-Tu Hsieh
Advised by James R. Goodman
Performance evaluation of the pipe computer architecture

Craig Sheppard Holt
Advised by James E. Smith
Diagnosis and self-diagnosis of digital systems
First employment at Tufts University

Implementing Precise Interrupts in Pipelined Processors
JAMES E. SMITH, and ANDREW R. PLESZKUN

Koujuch Liou
Advised by James R. Goodman
Design of pipelined memory systems for decoupled architectures

Gene M. Amdahl
Eckert-Mauchly Award
for
outstanding innovations in computer architecture, including pipelining, instruction look- ahead and cache memory

The Wisconsin Multicube: A New Large-Scale Cache-Coherent Multiprocessor
James R. Goodman and Philip J. Woest
Computer Sciences Department
University of Wisconsin-Madison

Evaluating Associativity in CPU Caches
MARK D. HILL, and ALAN JAY SMITH

Matthew K. Farrens
Advised by Andrew Pleszkun
The design and analysis of a high-performance single-chip processor
First employment at University of California, Davis

Richard E. Kessler
Advised by Mark D. Hill
Analysis of Multi-Megabyte Secondary CPU Cache Memories
First employment at Cray Research

CACHE CONSISTENCY AND SEQUENTIAL CONSISTENCY
by
James R. Goodman
Computer Sciences Technical Report #1006
February 1991

Fine-grain Access Control for Distributed Shared Memory*
Ioannis Schoinas, Babak Falsafi, Alvin R. Lebeck, Steven K. Reinhardt, James R. Larus, David A. Wood
Computer Sciences Department
University of Wisconsin–Madison
1210 West Dayton Street
Madison, WI 53706 USA
wwt@cs.wisc.edu

Sriram Vajapeyam
Advised by Gurindar S. Sohi
Instruction Level Characterization of the Cray Y-MP Processor
First employment at Cray Research

Dionisios Pnevm
Advised by Gurindar S. Sohi
Incorporating Guarded Execution into Existing Instruction Sets
First employment at FORTH-ICS

Ross Evan Johnson
Advised by James R. Goodman
Extending the scalable coherent interface for large-scale shared-memory multiprocessors
First employment at IBM

40 years of computer architecture research at University of Wisconsin-Madison

This poster highlights the professors, their PhD graduates, and some of the great works from the computer architecture program in the University of Wisconsin-Madison Computer Sciences department. Wisconsin computer architects have led the way through innovations in out-of-order processing, multi-CPU processing, transactional memory, branch predictors, caches, and many others. This poster is a window into the depth and breadth of this program.

Comments? Questions? Want to point out an error? Is your picture missing?
Email: powerjg@cs.wisc.edu

Poster designed by Jason Power (powerjg@cs.wisc.edu, pages.cs.wisc.edu/~powerjg)

Madhusudhan (Madhu) Talluri

Advised by Mark D. Hill

Use of Superpages and Subblocking in the Address Translation Hierarchy

First employment at Sun Microsystems

Trace Cache: a Low Latency Approach to High Bandwidth Instruction Fetching

Eric Rotenberg
Computer Science Dept.
Univ. of Wisconsin - Madison
ericro@cs.wisc.edu

Steve Bennett
Intel Corporation
sbennett@ichips.intel.com

James E. Smith
Dept. of Elec. and Comp. Engr.
Univ. of Wisconsin - Madison
jes@ece.wisc.edu

Abstract

As the issue width of superscalar processors is increased, instruction fetch bandwidth requirements will also increase. It will become necessary to fetch multiple basic blocks per cycle. Conventional instruction caches hinder this effort because long instruction sequences are not always in contiguous cache l

This paper appears in the 23rd International Symposium on Computer Architecture, May, 1996.

Reprinted by permi

Memory Bandwidth Limitations of Future Microprocessors

Doug Burger, James R. Goodman, and Alain Kägi

Computer Sciences Department
University of Wisconsin-Madison
1210 West Dayton Street
Madison, Wisconsin 53706 USA
galileo@cs.wisc.edu - http://www.cs.wisc.edu/~galileo

Andreas Moshovos

Advised by Gurindar S. Sohi

Memory Dependence Prediction

First employment at Northwestern University

Quinn Able Jacobson

Advised by James E. Smith

High-performance frontends for trace processors

First employment at Sun Microsystems

Eric Rotenberg

Advised by James E. Smith

Trace Processors: Exploiting Hierarchy and Speculation

First employment at NC State University

J. Adam Butts

Advised by Gurindar S. Sohi

Optimizing Inter-Instruction Value Communication through Degree of Use Prediction

First employment at IBM Research

Kevin Lep

Advised by Mikko

Exploring, Defin
Exploiting Recent S
Locality

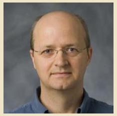
First employm
Advanced Micro

Alvin Lebeck

Advised by David A. Wood

Tools and Techniques for Memory System Design and Analysis

First employment at Duke University



The Predictability of Data Values

Yiannakis Sazeides and James E. Smith
rtment of Electrical and Computer Enginee
University of Wisconsin-Madison
1415 Engr. Dr.
Madison, WI 53706
{yanos,jes}@ece.wisc.edu

Ioannis (Yannis) Schoinas

Advised by Mark D. Hill

Fine Grain Distributed Shared Memory Systems on Clusters of Workstations

First employment at Intel Corporation

Subbarao Palacharla

Advised by James E. Smith

Complexity-effective superscalar processors

First employment at Intel

READINGS IN
Computer Architecture

EDITED BY
Mark D. Hill
Norman P. Jouppi
Gurindar S. Sohi

On the Value Locality of Store Instructions

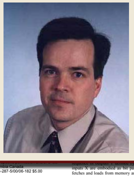
Kevin M. Lepak and Mikko H. Lipasti
Electrical and Computer Engineering
University of Wisconsin
1415 Engineering Drive
Madison, WI 53706
{lepak,mikko}@ece.wisc.edu

Abstract

Value locality, a recently discovered program attribute that describes the likelihood of the recurrence of previously-seen program values, has been studied enthusiastically in the recent published literature. Much of the

MIKKO H. LIPASTI

PhD Carnegie Mellon University



Daniel Sorin

Advised by David A. Wood

Using Lightweight Checkpoint/Recovery to Improve the Availability and Designability of Shared Memory Multiprocessors

First employment at Duke University

Adv
A
mach
d
Firs

Franklin

ohi
ure
son

Multiscalar Processors

Gurindar S. Sohi
sohi@cs.wisc.edu

Scott E. Breach
breach@cs.wisc.edu

T.N. Vijaykumar
vijay@cs.wisc.edu

Computer Sciences Department
University of Wisconsin-Madison
Madison, WI 53706

Steve Reinhardt

Advised by David A. Wood

Mechanisms for Distributed Shared Memory

First employment at University of Michigan

Shubhendu (Shubu) Mukherjee

Advised by Mark D. Hill

Design and Evaluation of Network Interfaces for System Area Networks

First employment at Digital Equipment Corporation

Alain Kagi

Advised by James R. Goodman

Mechanisms for efficient shared-memory, lock-based synchronization

First employment at Intel

JAMES E. SMITH
ECKERT-MAUCHLY AWARD

for

fundamental contributions to high performance micro-architecture, including saturating counters for branch prediction, reorder buffers for precise exceptions, decoupled access/execute architectures, and vector supercomputer organization memory, and interconnects.

1995

2000

Complexity-Effective Superscalar Processors

Subbarao Palacharla
Computer Sciences Department
University of Wisconsin-Madison
Madison, WI 53706, USA
subbarao@cs.wisc.edu

Norman P. Jouppi
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Digital Equipment Corporation
Palo Alto, CA 94301, USA
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J. E. Smith
Dept. of Electrical and Comput
University of Wisconsin-Ma
Madison, WI 53706, US
jes@ece.wisc.edu

Babak Falsafi

Advised by David A. Wood

Fine-Grain Protocol Execution Mechanisms & Scheduling Policies on SMP Clusters

First employment at Purdue University

Scott Breach

Advised by Gurindar S. Sohi

Design and Evaluation of a Multiscalar Processor

First employment at Compaq

Dynamic Speculation and Synchronization of Data Dependence

Andreas Moshovos, Scott E. Breach, T. N. Vijaykumar, Gurindar S. Sohi
Computer Sciences Department
University of Wisconsin-Madison
1210 West Dayton St.
Madison, WI 53706

GURINDAR S. SOHI
MAURICE WILKES AWARD

for

seminal contributions in the areas of high issue rate processors and instruction level parallelism

Avinash Sodani

Advised by Gurindar S. Sohi

Dynamic Instruction Reuse

First employment at Intel

natikatos

Billion-Tran
Architectures

Advances in semiconductor manufacturing will permit an unprec number of transistors on a single processor die. But what archite make the best use of these riches?

Doug Burger
James R. Goodman
University of Wisconsin-Madison

This paper appears in the 24th International Symposium on Computer Architecture, June, 1997.
Minor editorial changes: May 7, 1997.

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Efficient Synchronization: Let Them Eat QOLB[1]

Alain Kägi, Doug Burger, and James R. Goodman

Computer Sciences Department
University of Wisconsin-Madison
1210 West Dayton Street
Madison, Wisconsin 53706 USA
galileo@cs.wisc.edu - http://www.cs.wisc.edu/~galileo

Stefanos Kaxiras

Advised by James R. Goodman

Identification and optimization of sharing patterns for scalable shared-memory multiprocessors

First employment at Bell Labs

Trishul Chilimbi

Advised by Mark D. Hill and James R. Larus

Cache-Conscious Data Structures–Design and Implementation

First employment at Microsoft Corporation

Eric Schnarr

Advised by Mark D. Hill and James R. Larus

Applying Programming Language Implementation Techniques to Processor Simulation

First employment at Hypercosm Corporation

Amir Roth

Advised by Gurindar S. Sohi

Pre-Execution via Speculative Data-Driven Multithreading

First employment at University of Pennsylvania

Efficient Detection of All Pointer and Array Access Errors

Todd M. Austin Scott E. Breach Gurindar S. Sohi
Computer Sciences Department
University of Wisconsin-Madison
1210 W. Dayton Street
Madison, WI 53706
{austin, breach, sohi}@cs.wisc.edu

Dynamic Instruction Reuse

Avinash Sodani and Gurindar S. Sohi

Computer Sciences Department
University of Wisconsin-Madison
1210 West Dayton Street
Madison, WI 53706 USA
{sodani,sohi}@cs.wisc.edu

Sarita V. Adve

Advised by Mark D. Hill

Designing Memory Consistency Models for Shared-Memory Multiprocessors

First employment at Rice University

Todd Austin

Advised by Gurindar S. Sohi

Hardware and Software Mechanisms for Reducing Load Latency

First employment at Intel

Doug Burger

Advised by James R. Goodman

Hardware techniques to improve the performance of the processor/memory interface

First employment at University of Texas at Austin

EFFICIENT SYNCHRONIZATION PRIMITIVES FOR LARGE-SCALE CACHE-COHERENT MULTIPROCESSORS

James R. Goodman, Mary K. Vernon, and Philip J. Woest

T. N. Vijaykumar

Advised by Gurindar S. Sohi

Compiling for the Multiscalar Architecture

First employment at Purdue University

Appears in the proceedings of the Tenth International Conference on Architectural Support for Progra
Oct. 6-Oct. 9, 2002, San Jose, California.

Transactional Lock-Free Execution of Lock-Based Programs

Ravi Rajwar and James R. Goodman
Computer Sciences Department
University of Wisconsin-Madison

Anastasia (Natassa) Ailamaki

Advised by Mark D. Hill and David DeWitt

Architecture-Conscious Database Systems

First employment at Carnegie-Mellon University

Timothy Hume Heil

Advised by James E. Smith

Relational profiling in multithreaded virtual machines

First employment at IBM

oak
H. Lipasti
ing, and
tore Value
ent at
Devices

Milo Martin
Advised by Mark D. Hill
Token Coherence
First employment at
University of Pennsylvania

Alaa Alameldeen
Advised by David A. Wood
Using Compression to Improve Chip Multiprocessor Performance
First employment at Intel
Microprocessor Research Lab

Gordon Bell
Advised by Mikko H. Lipasti
Latency- and Error-Tolerant Redundant Execution
First employment at IBM

KARTHIKEYAN (KARU) SANKARALINGAM
PhD The University of Texas at Austin

Optimizing Throughput of Power- and Thermal-Constrained Multicore Processors Using DVFS and Per-Core Power-Gating
Jungseob Lee and Nam Sung Kim

LogTM: Log-based Transactional Memory
Kevin E. Moore, Jayaram Bobba, Michelle J. Moravan, Mark D. Hill & David A. Wood
Department of Computer Sciences, University of Wisconsin–Madison

MARK D. HILL
DISTINGUISHED SERVICE AWARD
for
leadership in improving the architecture community's review process, organizing computer architecture research information on-line, and providing outstanding service on the SIGARCH Executive Committee

Advised
Hardw
Efficient
Supervise
First em

Ho-Seop Kim
ised by James E. Smith
co-designed virtual
ine for instruction-level
istributed processing
t employment at Intel

STEVE SCOTT
MAURICE WILKES AWARD
for
For seminal contributions to the architecture and design of high-performance computer systems and interconnection networks

Harold (Trey) Cain
Advised by Mikko H. Lipasti
Detecting and Exploiting Causal Relationships in Hardware Shared-Memory Multiprocessors
First employment at
Qualcomm

SARITA ADVE
MAURICE WILKES AWARD
for
formalization of memory consistency models, especially data-race free models, and their influence on both hardware and high-level languages

Philip Wells
Advised by Gurindar S. Sohi
Dynamic Heterogeneity: Virtualization for the Multicore Era
First employment at Google

Kyle J. Nesbit
Advised by James E. Smith
Virtual Private Machines: A resource abstraction for multicore computer systems
First employment at Google

NAM SUNG KIM
PhD from University of Michig

Managing Wire Delay in Large Chip-Multiprocessor Caches
Bradford M. Beckmann and David A. Wood

Ilhyun Kim
Advised by Mikko H. Lipasti
Macro-op Scheduling and Execution
First employment at Intel

Ravi Rajwar
Advised by James R. Goodman
Speculation-based techniques for transactional lock-free execution of lock-based programs
First employment at Intel

Min Xu
Advised by Mark D. Hill and Rastislav Bodik
Race Recording for Multithreaded Deterministic Replay using Multiprocessor Hardware
First employment at VMware

Shiliang Hu
Advised by James E. Smith
Efficient binary translation in co-designed virtual machines
First employment at Intel

Kevin Moore
Advised by David A. Wood
Log-based Transactional Memory
First employment at Sun Microsystems Labs

Lixin Su
Advised by Mikko H. Lipasti
Streamlined atomic execution for Java
First employment at
Qualcomm

Nidhi Aggarwal
Advised by James E. Smith
Achieving high availability with commodity hardware and software
First employment at
McKinsey & Company

ANDREAS MOSHOVOS
MAURICE WILKES AWARD
for
foundational contributions to the area of mem dependence prediction

2005

Craig Zilles
Advised by Gurindar S. Sohi
Master/Slave Speculative Parallelization and Approximate Code
First employment at UIUC

DOUG BURGER
MAURICE WILKES AWARD
for
contributions to spatially distributed processor and memory systems architecture

Koushik Chakraborty
Advised by Gurindar S. Sohi
Over-provisioned Multicore Systems
First employment at Utah State University

SHUBU MUKHERJEE
MAURICE WILKES AWARD
for
outstanding contributions to modeling and design of soft-error tolerant microarchitectures

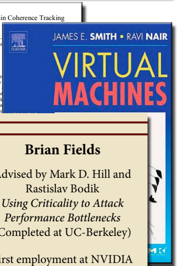
2010

GURINDAR S. SOHI
NATIONAL ACADEMY OF ENGINEERIN
COMPUTER SCIENCE
for
contributions to the design of high-performanc superscalar computer architectures

TODD AUSTIN
MAURICE WILKES AWARD
for
innovative contributions in Computer Architecture including the SimpleScalar Toolkit and the DIVA and Razor architectures

An Architectural Evaluation of Java TPC-W
Harold W. Cain, Ravi Rajwar, Morris Marden, Mikko H. Lipasti

Improving Multiprocessor Performance with Coarse-Grain Coherence Tracking
Jason F. Cantin, Mikko H. Lipasti, and James E.



Weaving Relations for Cache Performance
Anastassia Ailamaki, David J. DeWitt, Mark D. Hill, Marios Skounakis

Natalie Enright Jerger
Advised by Mikko H. Lipasti
Chip Multiprocessor Coherence and Interconnect System Design
First employment at University of Toronto ECE Dept

The gem5 Simulator

Jason F. Cantin
Advised by Mikko H. Lipasti
Coarse-grain coherence tracking
First employment at IBM

Brian Fields
Advised by Mark D. Hill and Rastislav Bodik
Using Criticality to Attack Performance Bottlenecks
(Completed at UC-Berkeley)
First employment at NVIDIA

Tejas Karkhanis
Advised by James E. Smith
Automated design of application-specific superscalar processors
First employment at AMD

Implementing Signatures for Transactional Memory
Daniel Sanchez, Luke Yen, Mark D. Hill, Karthikeyan Sankaralingam

Luke Yen
Advised by Mark D. Hill
Signatures in Transactional Memory Systems
First employment at AMD

Multifacet's General Execution-driven Multiprocessor Simulator (GEMS) Toolset

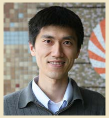
Virtual Circuit Tree Multicasting: A Case for On-Chip Hardware M

S. Subramanya Sastry
Advised by James E. Smith and Ras Bodik
Techniques for Transparent Program Specialization In Dynamic Optimizers
First employment at Environment Support Group, Bangalore

Brad Beckmann
Advised by David A. Wood
Managing Wire Delay in Chip Multiprocessor Caches
First employment at Microsoft Windows Server Performance

Ashutosh Sham Dhodapkar
Advised by James E. Smith
Autonomic management of adaptive microarchitectures
First employment at AMD

Jichuan Chang
Advised by Gurindar S. Sohi
Cooperative Caching for Chip Multiprocessors
First employment at HP Labs



Saisanthosh Balakrishnan
Advised by Gurindar S. Sohi
Program Demultiplexing: Data-flow Based Speculative Parallelization of Methods in Sequential Programs
First employment at Intel

Michael R. Marty
Advised by Mark D. Hill
Cache Coherence Techniques for Multicore Processors
First employment at Google

Eric Hill
Advised by Mikko H. Lipasti
Understanding and mitigating the effects of soft errors in logic
First employment at Intel

Jayaram Bobba

by Mark D. Hill

are Support for Transactional and d Memory Systems

ployment at Intel

LISHERS

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Daniel J. Sorin
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Andrew Nere

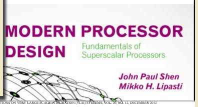
Advised by Mikko H. Lipasti

Computing with Hierarchical Attractors of Spiking Neurons

First employment at Thalchemy

Relax: An Architectural Framework for Software Recovery of Hardware Faults

Marc de Kruijf, Shuou Nomura, Karthikeyan Sankaralingam
Vertical Research Group
University of Wisconsin – Madison
{dekruijf, nomura, karu}@cs.wisc.edu



MODERN PROCESSOR DESIGN
Fundamentals of Superscalar Processors
John Paul Shen
Mikko H. Lipasti

IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 20, NO. 12, DECEMBER 2012

Analyzing the Impact of Joint Optimization of Cell Size, Redundancy, and ECC on Low-Voltage SRAM Array Total Area

am Sung Kim, Stark C. Draper, Shi-Ting Zhou, Sumeet Katariya, Hamid Reza Ghasemi, and Taejoon Park

---

Arkaprava (Arka) Basu

Advised by Mark D. Hill and Michael Swift

Revisiting Virtual Memory

First employment at AMD

Mitch Hayenga

Advised by Mikko H. Lipasti

Power-Efficient Loop Execution Techniques

First employment at ARM Inc.

Current Wisconsin Architecture Students

Chen-han Ho
Advised by Karu Sankaralingam

Marc Orr
Advised by David Wood

Sung Jin Kim
Advised by Karu Sankaralingam

Joel Hestness
Advised by David Wood and Steve Keckler

Tony Nowatzki
Advised by Karu Sankaralingam

Hamid Ghasemi
Advised by Nam Kim

Newsha Ardalani
Advised by Karu Sankaralingam

David Palframan
Advised by Nam Kim and Mikko Lipasti

Vijay Thiruvengadem
Advised by Karu Sankaralingam

Hao Wang
Advised by Nam Kim

Vinay Gangadhar
Advised by Karu Sankaralingam

Amin Farmahini
Advised by Nam Kim

Gagan Gupta
Advised by Guri Sohi

Zhenhong Liu
Advised by Nam Kim

Hongil Yoon
Advised by Guri Sohi

Ahmed Abulila
Advised by Nam Kim

Srinath Sridharan
Advised by Guri Sohi

Hadi Asgharimoghaddam
Advised by Nam Kim

Jayneel Gandhi
Advised by Mark Hill and Mike Swift

Michael Mishkin
Advised by Nam Kim

Jason Power
Advised by Mark Hill and David Wood

Paula Aguilera
Advised by Nam Kim

Lena Olson
Advised by Mark Hill

Mohammad Alian
Advised by Nam Kim

Chris Feilbach
Advised by Mark Hill

Anmol Mohanty
Advised by Nam Kim

Swapnil Haria
Advised by Mark Hill

Deahoon Kim (postdoc)
Advised by Nam Kim

Rathijit Sen
Advised by David Wood

Sean Franey
Advised by Mikko Lipasti

Somayeh Sardashti
Advised by David Wood

Arslan Zulfiqar
Advised by Mikko Lipasti

Muhammad Shoaib bin Atlaf
Advised by David Wood

Dibakar Gope
Advised by Mikko Lipasti

Nilay Vaish
Advised by David Wood

GURINDAR (GURI) SOHI
ECKERT-MAUCHLY AWARD

for

pioneering widely used micro-architectural techniques for instruction-level parallelism

YNTH
OMPU
ark D. Hi

JAMES R. GOODMAN
ECKERT-MAUCHLY AWARD

for

pioneering contributions to the architecture of shared-memory multiprocessors

---

Jungseob Lee

Advised by Nam Sung Kim

Optimizing Throughput and Power Consumption of Graphics Processing Units

First employment at Intel

GPUWattch†: Enabling Energy Optimizations in GPGPUs

Jingwen Leng[1], Tayler Hetherington[2], Ahmed ElTantawy[2], Syed Gilani[3], Nam Sung Kim[3], Tor M. Aamodt[2], Vijay Janapa Reddi[1]
[1] The University of Texas at Austin, [2] University of British Columbia, [3] University of Wisconsin-Madison

---

2011 International Conference on Parallel Architectures and Co

Improving Throughput of Power-Constrained GPUs Using Dynamic Voltage/Frequency and Core Scaling

Jungseob Lee[1], Vijay Sathisha[1], Michael Schulte[2], Katherine Compton[1], Nam Sung Kim[1]
[1]Department of Electrical and Computer Engineering, University of Wisconsin, Madison, WI, U.S.A.
[2]Advanced Micro Devices, Austin, TX, U.S.A.
e-mail: {jslee9, sathish}@wisc.edu, michael.schulte@amd.com, nskim3@wisc.edu

---

Erika Gunadi

Advised by Mikko H. Lipasti

CRIB: Consolidated Rename, Issue, and Bypass

First employment at Stealth Startup

ory

Yasuko Watanabe

Advised by David A. Wood

On Power Proportional Processors

First employment at AMD Research

Abhishek Sinkar

Advised by Nam Sung Kim

Improving Performance, Power Efficiency, Yield, and Reliability Using Programmable Power-gating Techniques

First employment at Oracle

Marc de Kruijf

Advised by Karu Sankaralingam

Compiler Construction of Idempotent Regions and Applications in Architecture Design

First employment at Google

Emily Blem

Advised by Karu Sankaralingam

Unified Models to Study Multicore Scaling Limits and Accelerator-based Solutions

First employment at Google

NG,

e,

Dan Gibson

Advised by David A. Wood

Scalable Cores in Chip Multiprocessors

First employment at Google Labs (Madison)

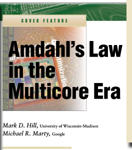
Atif Hashimi

Advised by Mikko H. Lipasti

Cortical Columns: A Non Von Neumann Computational Abstraction

First employment at Thalchemy

COVER FEATURE



Amdahl's Law in the Multicore Era

Mark D. Hill, University of Wisconsin-Madison
Michael R. Marty, Google

Augmenting Amdahl's law with a corollary for multicore hardware makes it relevant to future generations of chips with multiple processor cores. Obtaining optimal multicore performance will require further research in both extracting more parallelism and making sequential cores faster.

Daniel W. Chang

Advised by Nam Sung Kim and Michael Schulte

3D Stacked Memories for Digital Signal Processors

First employment at Rose-Hulman

Dark Silicon and the End of Multicore Scaling

Hadi Esmaeilzadeh† Emily Blem‡ Renée St. Amant§ Karthikeyan Sankaralingam‡ Doug Burger◇
†University of Washington ‡University of Wisconsin-Madison
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Matthew Allen

Advised by Gurindar S. Sohi

Data-Driven Decomposition of Sequential Programs for Determinate Parallel Execution

First employment at Amazon

KARTHIKEYAN SANKARALINGAM
YOUNG COMPUTER ARCHITECT AWARD

for

outstanding contributions in the field of computer architecture in both research and education

---

RAVI RAJWAR
MAURICE WILKES AWARD

for

contributions to the design and commercialization of hardware transactional memory

---

Dynamically Specialized Datapaths for Energy Efficient Computing

Venkatraman Govindaraju Chen-Han Ho Karthikeyan Sankaralingam
Vertical Research Group
Madison
cs.wisc.edu

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r GPGPU Spatial Multitasking

Jacob T. Adriaens, Katherine Compton, Nam Sung Kim
Department of Electrical and Computer Engineering
University of Wisconsin - Madison

Michael J. Schulte
AMD Research
Michael.Schulte@amd.com

Dana Vantrease

Advised by Mikko H. Lipasti

Optical Tokens in Many-core Processors

First employment at Qualcomm

Syed Gilani

Advised by Nam Sung Kim and Michael Schulte

Compute efficient embedded processors

First employment at AMD

Derek R. Hower

Advised by Mark D. Hill

Acoherent Shared Memory

First employment at AMD Postdoc

Venkatraman Govindaraju

Advised by Karu Sankaralingam

Energy Efficient Computing through Compiler Assisted Dynamic Specialization

First employment at Oracle