Partial Evaluation of Machine Code *

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Abstract
This paper presents an algorithm for off-line partial evaluation of machine code. The algorithm follows the classical two-phase approach of binding-time analysis (BTA) followed by specialization. However, machine-code partial evaluation presents a number of new challenges, and it was necessary to devise new techniques for use in each phase.

• Our BTA algorithm makes use of an instruction-rewriting method that “decouples” multiple updates performed by a single instruction. This method counters the cascading imprecision that would otherwise occur with a more naïve approach to BTA.

• Our specializer specializes an explicit representation of the semantics of an instruction, and emits residual code via machine-code synthesis. Moreover, to create code that allows the stack and heap to be at different positions at run-time than at specialization-time, the specializer represents specialization-time addresses using symbolic constants, and uses a symbolic state for specialization.

Our experiments show that our algorithm can be used to specialize binaries with respect to commonly used inputs to produce faster binaries, as well as to extract an executable component from a bloated binary.

Categories and Subject Descriptors F.3.2 [Semantics of Programming Languages]: Partial evaluation

Keywords Partial evaluation, machine code, BTA, specialization, machine-code synthesis, IA-32 instruction set

1. Introduction

The analysis and rewriting of binaries has gotten an increasing amount of attention from the academic community in the last decade (e.g., see references in [44, §7], [9, §1], [13, §1], [18, §7]). One of the potential applications of machine-code \(^1\) analysis and rewriting is to facilitate reuse of software binaries in the absence of source code. In particular, it would be desirable to have a binary-rewriting tool that can (i) optimize a binary for the common case (e.g., a file-write routine optimized for a certain file descriptor), or (ii) extract an executable component from a bloated binary (e.g., a small text encoder embedded in a web server).

Partial evaluation [25] is a program-specialization framework that can perform the aforementioned tasks. However, there are no tools that partially evaluate machine code. Existing binary-rewriting tools either de-obfuscate [16, 42, 47], superoptimize [11, 39], or harden [4, 20, 43] binaries, but do not perform partial evaluation. Moreover, machine-code partial evaluation presents a number of new challenges, and source-code partial-evaluation algorithms [6, 15, 26] would not produce satisfactory results if they were applied to machine code in a straightforward manner (see §3).

This paper presents an algorithm for off-line partial evaluation of machine code. The inputs to the algorithm are a binary B, and a division of B’s inputs as S (static inputs) and D (dynamic inputs). Values for static inputs are known at specialization time; values for dynamic inputs are unknown at specialization time. Our partial-evaluation algorithm produces a binary Bs that satisfies the equation

\[
[B](S, D) = [B_S](D),
\]

where \([\cdot]\) denotes the meaning function for the instruction set in which the binary is written. Executing Bs with input D produces the same results as executing B with inputs S and D. However, Bs is specialized with respect to S, and can be significantly faster than B.

Partially evaluating a binary with respect to commonly used inputs produces specialized versions of the binary that are optimized for the common inputs. (See §6.1.) Partially

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\(^1\) We use the term “machine code” to refer generically to low-level code, and do not distinguish between actual machine-code bits/bytes and assembly code to which it is disassembled.
evaluating with respect to a fixed value of an input flag can extract a smaller executable component from a bloated binary. (See §6.2.) The extracted component can be used in embedded systems where executable size matters, or be linked against other programs that require the component. (See the experiment with lzfx in §6.2.)

We have implemented our algorithm in a tool, called WiPER (an acronym for the “Wisconsin Partial Evaluator”), that partially evaluates Intel IA-32 binaries. WiPER works on the Intermediate Representations (IRs) recovered from machine code by an existing tool, CodeSurfer/x86 [10]. WiPER follows the classical two-phase approach of binding-time analysis (BTA) followed by specialization. WiPER’s BTA uses forward slicing to determine a priori which instructions can be specialized away (static instructions), and which cannot (dynamic instructions). Given the values for static inputs in the form of a partial state, WiPER’s specializer evaluates static instructions, residuates code for static values that might be used by dynamic instructions, and emits unmodified dynamic instructions.

As mentioned earlier, there are several new challenges that arise in the context of machine-code partial evaluation. These issues, along with the strategies that WiPER uses to overcome them, distinguish WiPER from other partial evaluators that have been described in the literature.

• Machine-code instructions are usually multi-assignments: they have several inputs, and several outputs (e.g., registers, flags, and memory locations). This aspect of the language introduces a granularity issue during slicing: in some cases, although we would like the slice to follow only a subset of an instruction’s semantics, the slicing algorithm is forced to include the entire instruction. This effect can cascade, and cause BTA to be very imprecise. The BTA algorithm in WiPER makes use of an instruction-rewriting method that decouples multiple updates performed by a single instruction by splitting the assignments across multiple instructions. The decoupling transformation increases the precision of WiPER’s BTA significantly.

• An instruction’s abstract-syntax tree (AST) is often not parameterized by all of the operands of the instruction: some operands are “baked into” the semantics. In contrast with source-code partial evaluators that specialize the AST of a dynamic statement, WiPER specializes an explicit representation of the semantics of a dynamic instruction, and uses a machine-code synthesizer [45] to produce residual code.

• In machine code, values in memory are accessed by explicit address computations, followed by loading. The residual code produced by a naïve machine-code partial evaluator will contain specialization-time addresses, and consequently would not allow the stack and heap to be at different positions at run-time than at specialization-time. WiPER represents specialization-time addresses using symbolic constants, and uses a symbolic state for specialization. The resulting code produced by WiPER is independent of the layout of the specialization-time address space, and can be run with, e.g., the stack base at a different address.²

The contributions of our work include the following:

• We present an algorithm for machine-code partial evaluation. To the best of our knowledge, WiPER is the first partial evaluator that works on machine code.³

• We have developed an instruction-decoupling transformation to counter cascading imprecision caused by the granularity issue in machine-code slicing.

• We have introduced an instruction-specialization technique that specializes an explicit representation of the semantics of an instruction with respect to a partial state, and residuates code via machine-code synthesis.

• We have developed a specialization algorithm that represents specialization-time addresses using symbolic constants, and uses a symbolic state for specialization. The residual code produced by our specializer is independent of the specialization-time memory layout, and allows the stack and heap to be at different positions at run-time than at specialization-time.

Our methods have been implemented in WiPER, a partial evaluator for Intel IA-32. We partially evaluated seven test applications using WiPER, and found that, on average (computed via geometric mean), the specialized binaries have a speedup of 1.3. We also used WiPER to extract executable components from bloated binaries such as bzip2.

2 Note that we are referring here to the ability to reposition the stack at the beginning of run-time, not the relocatability of the residual code per se. The residual code produced WiPER is also relocatable.

3 Confirmed by personal communication with Neil Jones, Robert Glück, and Saumya Debray.

2. Background

In this section, we briefly describe source-code partial evaluation, slicing, syntax and semantics of the IA-32 instruction-set architecture (ISA), and a logic to express the semantics of IA-32 instructions.

2.1 Partial Evaluation

Partial evaluation is a framework for specializing and optimizing programs [25]. Given a program that takes some inputs, and given values for some of the inputs, the goal of partial evaluation is to produce a program that is specialized (optimized) with respect to the input values provided. Fig. 1 shows a program power that computes \((a + b)^n\), where \(a\), \(b\), and \(n\) are the inputs to the program. Suppose that power is frequently called with the values \(b = 1\), and \(n = 4\). Given power, and the input values \(b = 1\) and \(n = 4\), a partial evaluator produces the residual program power\(_R\) shown in Fig. 2. As we can see in power\(_R\), partial evaluation has compiled data \((n = 4)\) into control. (See Eqn. (1).) In effect, partial evaluation performs optimizations such as loop unrolling,
int power(int a, int b, int n) { int prod = 1; 1: int prod = 1; 2: while (n--) { prod *= (a + 1); prod *= (a + 1); prod *= (a + 1); } 4: } 5: return prod; return prod; }

Figure 1: Input program. Computes \((a + b)^n\).

int foo() { 1: int a = 1, b = 2; 2: int c, d, e; 3: scanf("%d", &c); 4: d = add(a, b); 5: e = add(c, c); 6: return d + e; } int foo_r() { 1: int c, d, e; 2: scanf("%d", &c); 3: d = add(1, 2); 4: e = add(c, c); 5: return d + e; }

Figure 3: Example program foo to illustrate lifting.

Figure 2: Residual program. Computes \((a + 1)^4\).

Figure 4: Residual program.

Sometimes a static expression could be used in a dynamic
context. For example, consider the program foo given in
Fig. 3. Because c’s value is established dynamically in line
3, both of the formal parameters of add are classified dy-
namic by BTA. Although both actual parameters of the call
to add in line 4 of Fig. 3 are static, they appear in a dynamic
context—the static actuals will be bound to dynamic formals
in add. To produce a residual program that compiles and/or
does not access uninitialized locations, the partial evaluator
must residue code for the static actuals. Thus the partial
evaluator “lifts” static expressions that appear in dynamic
contexts, and the specializer residues code for lifted expres-
sions (e.g., line 3 in Fig. 4). The term “lifting” refers to the
process of changing the binding time of an expression
from static to dynamic.

Suppose that each statement in the original program is
uniquely identified by a label \(l\), and that each concrete state
\(\sigma\) that arises during an execution is partitioned into \(\sigma_S\) and
\(\sigma_D\) according to the division established by BTA. Then an execu-
tion trace of the original program is a sequence of
elements of the form \(l : (\sigma_S, \sigma_D)\). (Each element of the
trace records the state \((\sigma_S, \sigma_D)\) observed at an execution of a
statement \(l\).) The effect of partial evaluation on an execution
trace of the specialized program can be expressed by the
following reparenthesized:

\[
l : (\sigma_S, \sigma_D) \rightarrow (l, \sigma_S) : \sigma_D\tag{1}
\]

Operationally, the partial evaluator creates a new residual
statement for every unique \((l, \sigma_S)\) pair it observes at special-
ization time. Eqn. (1) shows how each element \((l, \sigma_S) : \sigma_D\)
in an execution trace of the specialized program can be mapped back to the corresponding element \(l : (\sigma_S, \sigma_D)\) in
the trace of the original program.

2.2 Slicing

Slicing [24, 46] computes the set of program points that af-
fect (or are affected by) a given program point called the
slicing criterion. (Backward slicing computes the set of pro-
gram points that might affect the slicing criterion; forward
slicing computes the set of program points that might be
affected by the slicing criterion.) Slicing is typically per-
fomed using an IR called a system dependence graph (SDG)
[21, 24]. An SDG consists of a set of program dependence
graphs (PDGs), one for each procedure in the program. A
node in a PDG corresponds to a construct in the program,
such as a statement, a condition, a call to a procedure, a
procedure entry/exit, an actual parameter of a call, or a formal
parameter of a procedure. The edges correspond to data and
control dependences between the nodes [21]. The PDGs are
connected together with interprocedural control-dependence
edges between call-site nodes and procedure-entry nodes,
and interprocedural data-dependence edges between actual
parameters and formal parameters/return values. Given an
SDG representation of the program and a slicing criterion,
an interprocedural-slicing algorithm includes in the slice the
INT ∈ Integer, Reg ∈ Register, I ∈ Instruction, O ∈ Operand,  
R ∈ RegisterOperand, C ∈ ImmediateOperand,  
M ∈ IndirectOperand, RC ∈ RegisterImmediateOperand  
INT ::= {..., -1, 0, 1, ...}  
Reg ::= eax | ebx | esp | ...  
R ::= Direct(Reg)  
C ::= Imm(INT)  
RC ::= R | C  
M ::= Indirect(R, R, INT)  
O ::= RC | M  
I ::= push(O) | mov(R, O) | mov(M, RC) | lea(R, M) |  
add(R, O) | add(M, RC) | sub(R, O) | sub(M, RC) |  
cmp(M, C) | jz(C) | jmp(C)  

Figure 5: Abstract syntax for a subset of IA-32.

SDG nodes that reach (or can be reached from) the slicing criterion by following data- and control-dependence edges. A context-sensitive interprocedural-slicing algorithm uses context-free language (CFL) reachability [35] to reduce the number of nodes in the slice [24, 36].

2.3 Syntax and Semantics of IA-32

Syntax. The abstract syntax for a subset of IA-32 instructions that will be used in this paper is given in Fig. 5. Indirect operands are of the form \langle base, index, scale, offset \rangle, where base and index are registers, and scale and offset are integers. The effective address is computed as base + index * scale + offset. In instructions with two operands, the operand on the left is the destination (except the cmp instruction, in which both operands are source operands).

Semantics. The primitive domains of the IA-32 semantics include 32-bit integers, Booleans, registers, and flags. The primitive domains and their operators are given below.

\[ i \in \mathbb{Z}_{32} \quad b \in \text{BOOL} = \{ \text{True}, \text{False} \} \]
\[ r \in \text{Register} = \{ \text{EAX}, \text{ESP}, \ldots \} \quad f \in \text{Flag} = \{ \text{CF}, \text{SF}, \ldots \} \]
\[ op \in \text{ArithOp} = \{ +, -, \ldots \} \quad \text{bop} \in \text{BoolOp} = \{ \land, \lor, \ldots \} \]
\[ \text{rop} \in \text{RelOp} = \{ =, \neq, <, \ldots \} \quad \text{cop} \in \text{CondOp} = \{ ? : \} \]

\text{Store} is a compound domain denoting an IA-32 store. \text{Store} is a triple consisting of three maps: a register map, a flag map, and a memory map. \text{Store} has operators to access and update the maps. The \text{Store} domain is defined below.

\[ \rho \in \text{Store} = \text{RegMap} \times \text{FlagMap} \times \text{MemMap} \]
\[ \text{RegMap} : \text{Reg} \rightarrow \text{INT} \]
\[ \text{FlagMap} : \text{Flag} \rightarrow \text{BOOL} \quad \text{MemMap} : \text{INT} \rightarrow \text{INT} \]

The valuation function \( \mathcal{I} \) has the type \( \mathcal{I} : \text{Instruction} \rightarrow \text{Store} \rightarrow \text{Store} \). \( \mathcal{I} \) takes an instruction \( I \) and a pre-store, and returns a post-store that reflects the updates made by the execution of \( I \). For example, the valuation function for the \text{mov eax, [ebp]} instruction is given below. The instruction copies a 32-bit value from the memory location pointed to by the frame-pointer register \text{EBP} to the \text{EAX} register. The overloaded function \( [\cdot] \) returns primitive semantic objects for their syntactic counterparts. The instruction also increments the program counter \text{EIP} by the length of the instruction. For brevity, we do not show this increment explicitly.

\[ T \in \text{Term}, \varphi \in \text{Formula}, FE \in \text{FuncExpr} \]
\[ c \in \text{Int32} = \{ \ldots, -1, 0, 1, \ldots \} \quad b \in \text{Bool} = \{ \text{True}, \text{False} \} \]
\[ I_{\text{Int32}} \in \text{Int32Id} = \{ \text{EAX}, \text{ESP}, \text{EBP}, \ldots \} \]
\[ I_{\text{Bool}} \in \text{BoolId} = \{ \text{CF}, \text{SF}, \ldots \} \quad F \in \text{FuncId} = \{ \text{Mem} \} \]
\[ op \in \text{ArithOp} = \{ +, -, \ldots \} \quad \text{bop} \in \text{BoolOp} = \{ \land, \lor, \ldots \} \]
\[ \text{rop} \in \text{RelOp} = \{ =, \neq, <, \ldots \} \]

\[ T ::= c | I_{\text{Int32}} | T_{1} op T_{2} | \text{ite}(\varphi, T_{1}, T_{2}) | F(T_{1}) \]
\[ \varphi ::= b | I_{\text{Bool}} | T_{1} rop T_{2} | \neg \varphi_{1} | \varphi_{1} \text{bop} \varphi_{2} | F = FE \]

\[ FE ::= F | FE_{1} T_{1} \mapsto T_{2} \]

Figure 6: Syntax of \( L[I_{32}] \).

\[ \mathcal{I}[\text{mov eax, [ebp]}] \rho = \text{update}_{\text{reg}}(\rho, [\text{eax}], \text{access}_{\text{mem}}(\rho, \text{access}_{\text{reg}}(\rho, [\text{ebp}]))) \]

2.4 QFBV Formulas for IA-32

The semantics of IA-32 instructions can also be formally expressed by formulas in a logic. Consider a quantifier-free bit-vector logic \( L \) over finite vocabularies of constant symbols and function symbols. We will be dealing with a specific instantiation of \( L \), denoted by \( L[I_{32}] \). \( L \) can also be instantiated for other ISAs in \( L[I_{32}] \), some constants represent IA-32’s registers (EAX, ESP, EBP, etc.), and some represent flags (CF, SF, etc.). \( L[I_{32}] \) has only one function symbol \"Mem\", which denotes memory. Note that syntactic constructs of \( L[I_{32}] \) are boldfaced to distinguish them from their counterparts in IA-32 semantics. The syntax of \( L[I_{32}] \) is defined in Fig. 6.

A term of the form \text{ite}(\varphi, T_{1}, T_{2}) represents an if-then-else expression. A \text{FuncExpr} of the form \( FE[T_{1} \mapsto T_{2}] \) denotes a function-update expression.

The function \( \langle \cdot \rangle \) converts an IA-32 instruction sequence into a QFBV formula. While others have created such encodings by hand (e.g., [38]), we use a method that takes a specification of the concrete operational semantics of IA-32 instructions and creates a QFBV encoder automatically. The method reinterprets each semantic operator as a QFBV formula-constructor or term-constructor. (See [30].) To write formulas that express store transitions, all \text{Int32Ids}, \text{BoolIds}, and \text{FuncIds} can be qualified by primes (e.g., \text{Mem}'). The QFBV formula for an instruction sequence is a restricted 2-vocabulary formula that specifies a store transformation (also known as a \text{transition formula}). It has the form

\[ \bigwedge_{m} (I'_{m} = T_{m}) \land \bigwedge_{n} (J'_{n} = \varphi_{n}) \land \text{Mem'} = FE, \]

where \( I'_{m} \) and \( J'_{n} \) range over the constant symbols for registers and flags, respectively. The primed vocabulary is the post-store vocabulary, and the unprimed vocabulary is the pre-store vocabulary. We also refer to them as \"vocabulary 1\" and \"vocabulary 0\", respectively. The QFBV formulas for a few IA-32 instructions are given in Fig. 7. The second instruction pushes the 32-bit constant value 0 on the stack. If the zero flag ZF is set, the third instruction updates EIP
to the value 1000; otherwise, it increments EIP by four. The fourth instruction loads EAX with the value EBP+4 (without modifying the value of any flag).

In this section, and in the rest of the paper, we show only the portions of QFBV formulas that express how the store is modified. QFBV formulas actually contain identity conjuncts of the form \( I = J \) and \( M = \text{Mem} \) for constants and functions that are unmodified.

3. Overview

At a very high level, WiPER is similar to the off-line source-code partial evaluator described in §2.1: WiPER’s algorithm works in two phases, BTA and specialization. However, because WiPER is dealing with machine code, WiPER’s algorithm differs significantly from that of a source-code partial evaluator. In this section, we present an example to illustrate WiPER’s algorithm, while highlighting the following: (i) the issues that arise in machine code, (ii) why techniques used in a source-code partial evaluator are unsatisfactory to resolve the issues, and (iii) how WiPER resolves the issues.

Fig. 8 shows an IA-32 program \( \text{sum} \) that takes, \( a, v \), and \( n \) as inputs, and computes \( a + b[n] \). (Array \( b \) is statically allocated and has 5 elements. Lines 6–12 in Fig. 8 initialize the elements of \( b \).) \( n \) is assumed to be between 0 and 4. The inputs \( a, v \), and \( n \) are available in the \( \text{eax} \), \( \text{ebx} \), and \( \text{ecx} \) registers, respectively, at the beginning of the program.

The output is available in the \( \text{eax} \) register at the end of the program. Let us use WiPER to partially evaluate \( \text{sum} \) with respect to the input value \( v = 1 \).

No source-code variables. Recall from §2.1 that the goal of BTA is to compute the division of all program variables as either static or dynamic. The abstraction of a source-code “variable” is absent at the machine-code level. (We assume that the input binary lacks symbol-table and debugging information.) Consequently, a division of source-code variables cannot be obtained at the machine-code level.

However, there are tools [10] that recover “variable-like” abstractions [9] from machine code, and use them to construct IRs such as an SDG, a control flow graph (CFG), etc. WiPER performs BTA via forward slicing over the SDG recovered from the binary [17].

The inputs to WiPER’s BTA phase are: (i) the SDG of the binary, and (ii) the instructions that initialize the dynamic inputs (the slicing criterion). The output is an annotated program, whose instructions are annotated with binding times: static (S), or dynamic (D). In our example, the dynamic inputs \( a \) and \( n \) are available in the \( \text{eax} \) and \( \text{ecx} \) registers at in-

\[
\begin{align*}
\text{mov} \text{eax},[\text{ebp}] & \equiv EAX' = \text{Mem}(\text{EBP}) \\
\text{mov} \text{eax},[\text{ebx}] & \equiv ESP' = ESP - 4 \wedge \text{Mem}' = \text{Mem}(\text{ESP} - 4 \rightarrow 0) \\
\text{jz} 1000 & \equiv \text{ite}(ZF = 0, \text{EIFP}' = 1000, \text{EIFP}' = \text{EIFP}) \\
\text{lea} \text{eax},[\text{ebx}+4] & \equiv EAX' = \text{EIFP} + 4
\end{align*}
\]

Figure 7: QFBV formulas for example IA-32 instructions.

\[
\begin{align*}
1: \text{push} \text{eax}, a & \quad 10: \text{mov} [\text{esp}+\text{edx}+4], \text{ebx} \\
2: \text{push} \text{ebx}, v & \quad 11: \text{sub} [\text{esp}+20], 1 \\
3: \text{push} \text{ecx}, n & \quad 12: \text{jmp} \text{L2} \\
4: \text{push} 4 & \quad 13: \text{L1:mov} \text{eax},[\text{esp}+32] \\
5: \text{sub} \text{esp},20 & \quad 14: \text{mov} \text{ecx},[\text{esp}+24] \\
6: \text{cmp} [\text{esp}+20],0 & \quad 15: \text{mov} \text{ebx},[\text{esp}+\text{ecx}+4] \\
7: \text{jl} \text{L1} & \quad 16: \text{add} \text{eax}, \text{ebx} \\
8: \text{mov} \text{ebx},[\text{esp}+28] & \quad 17: \text{add} \text{esp},36
\end{align*}
\]

Figure 8: Input \( \text{sum} \) program, which computes \( a + b[n] \).

\[
\begin{align*}
1: \text{push} \text{eax}, \text{ebx}, \text{ecx} & \quad 9: \text{mov} \text{edx},[\text{esp}+20] \\
2: \text{push} \text{ebx} & \quad 10: \text{mov} [\text{esp}+\text{edx}+4], \text{ebx} \\
3: \text{push} \text{ecx}, \text{edx} & \quad 11: \text{sub} [\text{esp}+20], 1 \\
4: \text{push} 4 & \quad 12: \text{jmp} \text{L2} \\
5: \text{sub} \text{esp},20 & \quad 13: \text{L1:mov} \text{eax},[\text{esp}+32] \\
6: \text{cmp} [\text{esp}+20],0 & \quad 14: \text{mov} \text{ecx},[\text{esp}+24] \\
7: \text{jl} \text{L1} & \quad 15: \text{mov} \text{ebx},[\text{esp}+\text{ecx}+4] \\
8: \text{mov} \text{ebx},[\text{esp}+28] & \quad 16: \text{add} \text{eax}, \text{ebx} \\
10: \text{lea} [\text{esp}+4] & \quad 17: \text{add} \text{esp},36
\end{align*}
\]

Figure 9: SDG snippet to illustrate decoupling.

The granularity issue in slicing. Consider instruction 1 in the \( \text{sum} \) program. 1 modifies the stack-pointer register \( \text{EIFP} \) in addition to copying the value in the \( \text{EAX} \) register to a memory location. Because all of the remaining instructions in \( \text{sum} \) either directly or transitively use \( \text{EIFP} \), the slice with respect to instruction 1 consists of all the instructions in \( \text{sum} \), and thus every instruction in \( \text{sum} \) would be classified dynamic. This imprecision in slicing is caused by a granularity problem: the \( \text{push} \) instruction independently updates \( \text{EIFP} \) and the memory location. Because the dynamic input is in \( \text{EIFP} \), the slice requires only the memory update that \( \text{push} \) performs and not the update to the value of \( \text{EIFP} \). However, a slice cannot include only a part of an instruction; it has to include the entire instruction. Consequently, the entire \( \text{push} \) instruction, and the remaining instructions in \( \text{sum} \) are added to the slice. This issue is illustrated by the SDG snippet on the left in Fig. 9.

To resolve this issue, WiPER rewrites \( \text{sum} \) by decoupling each instruction that independently updates the stack pointer along with another register or memory location \( l \) (e.g., \( \text{push}, \text{pop}, \text{leave} \), etc.). For such instructions, WiPER uses a machine-code synthesizer [45] (a tool that synthesizes an instruction sequence from a semantic specification) to synthe-
size an equivalent instruction sequence that updates ESP in one instruction and \( l \) in a different instruction. The effect of decoupling on BTA is illustrated by the SDG snippet on the right in Fig. 9.

The rewritten binary \( \sum' \) is shown in Fig. 10. In \( \sum' \), the new slicing criterion includes instructions \( z' \) and \( o' \). The new forward slice includes only the instructions highlighted in Fig. 10 in light gray, which are classified dynamic. The remaining instructions are classified static.

The inputs to the specialization phase of \( \text{WiPER} \) are: (i) the interprocedural CFG of the binary, (ii) the binding-time annotations, and (iii) an input partial static-store. The output is the residual program. Recall from \S 2.3 that an IA-32 store is a triple that consists of a register map, a flag map, and a memory map. The input partial static-store \( \rho_0 \) is

\[
\rho_0 \equiv \langle \text{ESP} \mapsto 1000 \rangle \langle \text{EBX} \mapsto I \rangle \langle [], [] \rangle.
\]

In the rest of the paper, when we use the term “store,” we are referring to a partial static-store. The input store has the value \( I \) for \( v \), and \( 1000 \) for the stack pointer. Let us specialize \( \sum' \) with respect to \( \rho_0 \).

**Non-parameterized operands in Instruction ASTs.** Recall from \S 2.1 that \( PE_S \) substitutes values for operands while specializing ASTs of dynamic expressions and statements. However, \( \text{WiPER} \) cannot use this simple approach for specializing dynamic instructions. For an instruction that has multiple input operands, the instruction AST may not always be parameterized by all operands. For example, the instruction \( \text{adc eax, ebx} \) adds the values in registers \( EAX \) and \( EBX \), and the value of the carry flag \( CF \). The flag operand is “baked into” the semantics, and is not an explicit syntactic operand. Another example is the instruction \( \text{push eax, ebx} \), which has the stack-pointer operand \( (ESP) \) baked into the semantics.

To handle this issue, \( \text{WiPER} \) specializes a representation of the semantics of an instruction—instead of its syntax—with respect to a store. \( \text{WiPER} \) uses a QFBV formula to represent an instruction’s semantics.

Now let us use the following approach to specialization:

1. Static instructions: Evaluate.
2. Dynamic instructions: Specialize the instruction’s QFBV formula with respect to the pre-store, and residuate code. \( \text{WiPER} \) uses a machine-code synthesizer to synthesize an instruction-sequence that is equivalent to the specialized QFBV formula. The synthesized instruction-sequence constitutes the residual code.

Let us specialize \( \sum' \) with respect to \( \rho_0 \) using this simple approach. The specializer evaluates instruction \( 1' \) in \( \sum' \) because it is static. The post-store is \( \rho_1 \).

\[
\rho_1 \equiv \langle \text{ESP} \mapsto 996 \rangle \langle \text{EBX} \mapsto I \rangle \langle [], [] \rangle.
\]

The QFBV formula for instruction \( z' \) is

\[
\langle \langle z' \rangle \rangle \equiv \text{Mem}' = \text{Mem}[\text{ESP} \mapsto EAX],
\]

Because \( z' \) is dynamic, the specializer specializes \( \langle \langle z' \rangle \rangle \) with respect to \( \rho_1 \) to obtain the specialized formula

\[
\text{Mem}' = \text{Mem}[996 \mapsto EAX],
\]

and uses the synthesizer to synthesize the instruction \( \text{mov [996], eax} \). After evaluating static instructions \( 3' \) and \( 4' \), the resulting store is

\[
\rho_4 \equiv \langle \langle \text{ESP} \mapsto 992 \rangle \langle \text{EBX} \mapsto I \rangle \langle [], [992, 992 \mapsto I] \rangle.
\]

The residual program produced by this simple approach is given below.

<table>
<thead>
<tr>
<th>Instruction 1</th>
<th>Instruction 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>mov [996], eax</td>
<td>mov ecx, [988]</td>
</tr>
<tr>
<td>mov [988], ecx</td>
<td>mov ebx, [964+ecx×4]</td>
</tr>
<tr>
<td>mov eax, [996]</td>
<td>add eax, ebx</td>
</tr>
</tbody>
</table>

**Lifting.** The approach described above produces code that can access uninitialized locations. For example, one can see that the instruction “mov ebx, [964+ecx×4]” in the residual program dereferences a dynamic pointer to access an element in the static array \( b \). However, the static array is not initialized by the residual code. This issue arises because our simple specialization approach did not residuate code for static instructions that produce values that might be consumed by a downstream dynamic instruction (a.k.a., a dynamic context).

To resolve this issue, \( \text{WiPER} \) conservatively lifts static predecessors of a dynamic instruction. In Fig. 10, the boxed instructions are the lifted instructions. After lifted instructions are identified, one can use the following approach to specialization:

**Approach \( PE_1 \):**

- Static instructions: Evaluate.
- Lifted instructions: Specialize the instruction’s QFBV formula with respect to the pre-store, and residuate code. Then update the store by evaluating the instruction.
- Dynamic instructions: Emit. Because all static locations that might be used by a dynamic instruction \( d \) have been initialized by upstream residual lifted instructions, there is no static data that needs to be infused into \( d \) via specialization, and the unmodified \( d \) can be emitted.
Let us specialize $\sum'$ with respect to $\rho_0$ using $\text{PE}_1$. Because $1'$ is lifted, the specializer residuates code for it. The QFBV formula for $1'$ is $\langle 1' \rangle \equiv \text{ESP'} = \text{ESP} - 4$. The specializer specializes $\langle 1' \rangle$ with respect to $\rho_0$ to obtain the specialized formula $\text{ESP'} = 996$, and uses the synthesizer to synthesize instruction $1_1$ in $\sum_1$ (shown in Fig. 11). The specializer also evaluates $1'$ to obtain $\rho_1$ (Eqn. (2)). Because $2'$ is dynamic, the specializer emits it as $2_1$. Because $3'$ is static, the specializer evaluates the instruction without residuating code. The new residual program $\sum_1$ is shown in Fig. 11. In $\sum_1$, one can see that all the static value required by emitted dynamic instructions ($2_1$, $6_1$, etc.) have been set up by residual lifted instructions ($1_1$, $5_1$, etc.).

Residual specialization-time addresses. In $\sum_1$, one can see that the specialization-time values of the stack pointer have been residuated as constants. Although $\sum_1$ is a correct residual program for $\sum'$ partially evaluated with respect to $\rho_0$, the specialization-time stack layout is hard-wired into the residual code. (The stack begins at address 1000, and grows toward lower addresses.) As a result, the residual code might crash if a different address is used as the base of the runtime stack.

One way to prevent the specializer from emitting stack-pointer values is to make the stack pointer dynamic by including instruction $1'$ in the slicing criterion during BTA. However, that would make all instructions in $\sum'$ dynamic.

To resolve this issue, $\text{WiPER}$ uses a symbolic store during specialization, instead of a concrete store. In the initial symbolic store, specialization-time addresses (e.g., the initial value of ESP) are represented using symbolic constants. Static non-address values are represented using integer and Boolean constants. $\text{WiPER}$ uses $\text{PE}_2$ for specialization.

Approach $\text{PE}_2$

- Static instructions: Symbolically evaluate. Although specialization-time addresses are symbolic, $\text{WiPER}$ can still access and update static values in memory.
- Lifted instructions: Specialize the instruction’s QFBV formula with respect to the symbolic pre-store, and residuate code. Then update the symbolic store by symbolically executing the instruction.
- Dynamic instructions: Emit.

Let us illustrate $\text{PE}_2$ on $\sum'$. The new initial store is $\rho_0^{sym} \equiv \langle \text{ESP} \mapsto c \mid \text{EBX} \mapsto l \rangle$. Note that the values in the store are boldface to indicate that they are logical terms, and not semantic values. The value of the stack pointer ESP is the symbolic constant $c$ to indicate that we are not restricting ESP to a concrete value known at specialization-time.

Before starting specialization, $\text{WiPER}$ residuates instruction $0_2$ in $\sum_2$ (shown in Fig. 12) to save the initial value of the stack pointer ESP in a dedicated location. (In this example, $\text{WiPER}$ uses the ESI register because ESI is not used in $\sum'$.) This location will be used whenever downstream residual instructions need the initial value of ESP. To residuate code for the lifted instruction $1'$, $\text{WiPER}$ specializes $\langle 1' \rangle$ with respect to $\rho_0^{sym}$. The specialized formula is $\text{ESP'} = c - 4$. Because at run-time the value of $c$ will be available in ESI, $\text{WiPER}$ replaces $c$ with ESI to produce $\text{ESP'} = \text{ESI} - 4$. $\text{WiPER}$ uses the synthesizer to synthesize instruction $1_2$ for the specialized formula. $\text{WiPER}$ also symbolically evaluates $1'$ to produce $\rho_1^{sym}$.

$$\rho_1^{sym} \equiv \langle \text{ESP} \mapsto c - 4 \mid \text{EBX} \mapsto l \rangle.$$  

$2'$ is dynamic, and $\text{WiPER}$ emits it as $2_2$. After symbolically evaluating static instructions $3'$ and $4'$, we obtain the store $\rho_2^{sym} \equiv \langle \text{ESP} \mapsto c - 8 \mid \text{EBX} \mapsto l \rangle$.

The final residual program $\sum_2$ produced by $\text{WiPER}$ is shown in Fig. 12. One can see that $\text{WiPER}$ arranges for the initial stack-pointer value to be retrieved from ESI ($1_2$, $5_2$, $9_2$, $13_2$, etc.) instead of residuating the stack-pointer value at residual lifted instructions (cf. $1_1$, $5_1$, $9_1$, $13_1$, etc. in $\sum_1$); consequently, $\sum_2$ will not crash when the stack base is initialized to different addresses. In contrast, static non-address quantities are residuated at lifted instructions (e.g., the value 1 in instructions $13_2$ through $13_5$).

Why do $\text{PE}_1$ and $\text{PE}_2$ work? To formalize the effect of $\text{PE}_1$ and $\text{PE}_2$, we introduce the notion of an environment, which makes explicit the starting address of the stack and heap blocks. An environment maps a symbolic constant denoting the starting address of the stack or a heap block to a concrete address (or “location”). A machine-code state $\sigma$ consists of an environment $\eta$, and a store $\rho$, which maps locations to values. For example, $\rho_4$ in Eqn. (3) is actually part of a state $\sigma_4$.

$$\sigma_4 \equiv \langle \eta_4, \rho_4 \rangle \equiv \langle \text{Stack} \mapsto 1000, \langle \text{ESP} \mapsto 992 \mid \text{EBX} \mapsto l \rangle, \{\text{ESP} \mapsto 992 \mid \text{EBX} \mapsto l\}\rangle.$$  

$\eta_4$ maps the start of the stack, denoted by the symbolic constant $\text{Stack}$, to the address 1000. Suppose that $\eta$ and $\rho$ can be partitioned into $\eta_S$ and $\eta_D$, and $\rho_S$ and $\rho_D$, respectively. The effect of $\text{PE}_1$ on...
Algorithm 1 Instruction Decoupling (Pre-processing step)

Input: Binary B
Output: Rewritten binary B’
1: for each i ∈ B do
2: if UpdatesSPAndLoc(i) then
3: I ← InstrToQFBV(i)
4: B’ ← Replace(B, i, I)
5: end if
6: end for
7: return B’

Algorithm 2 BTA algorithm in WiPER

Input: SDG, I₀
Output: BTAMap
1: slice ← ForwardSlice(SDG, I₀)
2: for each I ∈ slice do
3: BTAMap ← BTAMap[I → Dynamic]
4: for each static predecessor S of I do
5: BTAMap ← BTAMap[S → Lifted]
6: end for
7: end for
8: for each I ∈ Dom(BTAMap) do
9: if I is a call to malloc or an actual argument of a call to malloc then
10: BTAMap ← BTAMap[I → Lifted]
11: else
12: BTAMap ← BTAMap[I → Static]
13: end if
14: end for
15: return BTAMap

each execution trace of the binary can be expressed by the following reparenthesization:

\[ I : (\eta_S, \rho_S, \eta_D, \rho_D) \rightarrow (l, \eta_S, \rho_S) : (\eta_D, \rho_D) \]  

(4)

Operationally, the partial evaluator creates a new residual instruction for every unique \((I, \eta_S, \rho_S)\) triple it observes at specialization time. Eqn. (4) shows how each element \((I, \eta_S, \rho_S) : (\eta_D, \rho_D)\) in an execution trace of a binary specialized using PE₁ can be mapped back to the corresponding element \((l, \eta_S, \rho_S, \eta_D, \rho_D)\) in the trace of the original binary. Consequently, the specialization-time memory layout \((\eta_S)\) is hard-wired into the residual code. If the run-time memory layout is different, the residual code produced by PE₁ might crash.

To describe the symbolic techniques used in PE₂, we introduce a static symbolic store \(\rho_S^{sym}\), which maps symbolic expressions to symbolic expressions, where each such symbolic expression is parameterized on the symbolic constants found in \(\eta_S\). (Note that the domain of \(\rho_S^{sym}\) also contains registers and flags.) \(\rho_S^{sym}\) mirrors the static concrete store \(\rho_S\), i.e., \([\rho_S^{sym}][\eta_S] = \rho_S\), where the left-hand side denotes the simplification of each symbolic expression in \(\rho_S^{sym}\) with respect to the values obtained from \(\eta_S\). The principal effect of PE₂ on each execution trace of the binary can be expressed by the following reparenthesization:

\[ I : (\eta_S, \rho_S, \eta_D, \rho_D) \rightarrow (l, \rho_S^{sym}) : (\eta_S, \eta_D, \rho_D) \]  

(5)

Eqn. (5) shows how each element \((l, \rho_S^{sym}) : (\eta_S, \eta_D, \rho_D)\) in an execution trace of a binary specialized using PE₂ can be mapped back to the corresponding element \((l : (\eta_S, \rho_S, \eta_D, \rho_D)\) in the trace of the original binary. In effect, the residual code is independent of \(\eta_S\). (See also §4.4.)

4. Algorithm

In this section, we describe the algorithms used by WiPER. First, we present the algorithm for a pre-processing step used prior to partial evaluation. Second, we present WiPER’s intraprocedural partial-evaluation algorithm. Third, we present extensions to handle multiple procedures. Finally, we present the threats to the validity of our algorithms.

4.1 Pre-processing: Decoupling Instructions

Prior to performing BTA, WiPER rewrites the input binary by decoupling each instruction \(i\) that updates the stack-pointer register ESP along with another location \(l\). WiPER uses the machine-code synthesizer MCSYNTH [45] for decoupling. MCSYNTH uses a divide-and-conquer strategy that splits \(i\)’s QFBV formula \(\phi\) into two independent subformulas \(\phi_1\) and \(\phi_2\), such that the updates to ESP and \(l\) are split between \(\phi_1\) and \(\phi_2\). Then, MCSYNTH synthesizes code for \(\phi_1\) and \(\phi_2\), concatenates the results, and returns the resulting instruction sequence \(l\). ESP and \(l\) are updated in different instructions in \(I\). The rewriting of the input binary via instruction decoupling is shown as Alg. 1. In the algorithm, UpdatesSPAndLoc returns true if an instruction updates the stack pointer along with another register or memory location; InstrToQFBV converts an instruction into a QFBV formula; Synth invokes MCSYNTH to synthesize an instruction sequence; Replace replaces an instruction in a binary with an instruction sequence.

4.2 Intraprocedural Partial Evaluation

In this section, we present WiPER’s intraprocedural partial-evaluation algorithm. First, we present the BTA algorithm; then, we present the specialization algorithm.

4.2.1 BTA

The slicing-based BTA algorithm used in WiPER is shown as Alg. 2. In the algorithm, \(I_D\) is the set of instructions that initialize dynamic inputs; ForwardSlice computes a forward slice with respect to a slicing criterion; BTAMap is a data structure that maps each instruction to its binding time. If a static instruction is control dependent on a dynamic branch, the specialization algorithm might not terminate [25, Chap. 14]. To avoid the possibility of non-termination, ForwardSlice follows both data and control dependences during slicing. Lines 4–6 in Alg. 2 show the computation of lifted instructions during BTA. WiPER lifts all static calls to malloc (lines 9–11). This step is performed so that heap blocks that are allocated at specialization-time also get allocated at run-time. (See §4.2.2.3.)
4.2.2 Specialization

This section presents the specialization algorithm used in WiPER. We first present the skeleton of WiPER’s specialization loop. We then present two versions of the core specialization function specialize, which gets called in the specialization loop. While the first version produces correct residual code, the residual code cannot be executed with the stack and heap blocks at different positions at run-time than at specialization-time. The second version does not have this limitation, and is used in WiPER.

4.2.2.1 Specialization loop. The skeleton of WiPER’s specialization loop is similar to that of a standard partial evaluator [25, p. 87], and is given as Alg. 3. specialize is the core specialization function (line 13 of Alg. 3), which specializes an instruction with respect to a pre-store to obtain the residual instruction and a post-store. In the algorithm, $\epsilon$ denotes the empty sequence of instructions; NewCFG creates a new CFG; FirstBB returns the first basic-block in a CFG; FinalBB returns true if the argument is the final basic-block in its parent CFG; RemoveItem removes an item from the worklist; Emit appends an instruction to a CFG. (We assume that Emit creates and connects nodes in the CFG.)

Recall that the register EIP is the IA-32 program counter. Alg. 3 follows CFG edges, rather than the value of EIP, because we have no way to give consistent EIP values to new instructions created via decoupling. Alg. 3 does not even track EIP in stores, and consequently, it can propagate the same store to the two successors of a branch instruction (lines 21–23).

4.2.2.2 PE₁ Specializer. specialize₁ is a specialization function that implements PE₁. specialize₁ has two constituent functions, eval₁ and reduce₁. eval₁ evaluates instructions, and reduce₁ residues code. The algorithm for specialize₁ is given as Alg. 4.

**Algorithm 3 WiPER’s specialization loop - IntraPE**

**Input:** CFG, $\rho$, BTAMap  
**Output:** $\rho'$

1. CFG $\leftarrow$ NewCFG()  
2. bb $\leftarrow$ CFG.FirstBB()  
3. worklist $\leftarrow$ {bb, $\rho$}  
4. processed $\leftarrow$ $\emptyset$  
5. $\rho' \leftarrow \rho$  
6. while worklist $\neq \emptyset$ do  
7. (bb, $\rho$) $\leftarrow$ RemoveItem(worklist)  
8. if (bb, $\rho$) $\in$ processed then  
9. continue  
10. end if  
11. processed $\leftarrow$ processed $\cup$ {bb, $\rho$}  
12. for each instruction i $\in$ bb do  
13. (i', $\rho$) $\leftarrow$ specialize(i, $\rho$, BTAMap)  
14. if i' $\neq$ $\epsilon$ then  
15. CFG.Emit(i')  
16. end if  
17. end for  
18. if CFG.FinalBB(bb) then  
19. $\rho' \leftarrow \rho$  
20. end if  
21. for each successor s of bb do  
22. worklist $\leftarrow$ worklist $\cup$ {(s, $\rho$)}  
23. end for  
24. end while  
25. return $\rho'$

**Algorithm 4 specialize₁**

**Input:** I, $\rho$, BTAMap  
**Output:** ($I'$, $\rho'$)

1. if BTAMap[I] = Dynamic then  
2. return (I, $\rho$)  
3. else if BTAMap[I] = Lifted then  
4. return (reduce₁(I, $\rho$), eval₁(I, $\rho$))  
5. else  
6. return ($\epsilon$, eval₁(I, $\rho$))  
7. end if

For example, suppose that I is the instruction “add [esp], eax.” I’s QF BV formula $\varphi$ is given below. (For brevity, we only show one of the flags updated by add.)

$$\varphi \equiv \text{Mem}' = \text{Mem}[\text{ESP} \mapsto \text{Mem}(\text{ESP}) + \text{EAX}] \land \text{SF}' = (\text{Mem}(\text{ESP}) + \text{EAX} < 0)$$

Suppose that $\rho$ is $\rho = ([\text{ESP} \mapsto 1000][\text{EAX} \mapsto 2], \epsilon, [1000 \mapsto 1]).$ Subst₀ produces the following formula:

$$\text{Mem}' = \text{Mem}(1000) \mapsto 3 \land \text{SF}' = \text{False}.$$
4.2.2.3 PE2 specializer. As discussed in §3, Alg. 4 specializes the binary with respect to static addresses as well as static values (e.g., \( \text{sum}_1 \) in Fig. 11). In this section, we present the specialization algorithm that WiPER uses to resituate code that is independent of the specialization-time memory layout. In particular, we illustrate how the algorithm generates a residual program that allows the stack and heap blocks to be at different positions at run-time than at specialization-time.

WiPER’s call-graph is represented in Fig. 13. WiPER’s specializer is highlighted in Fig. 13 in light gray. WiPER uses specialize\(_2\) (Alg. 5) as the specialization function in Alg. 3. specialize\(_2\) implements PE\(_2\). The remaining components of the specializer (Algs. 6, 7, and 8) will be described later in upcoming paragraphs and sections.

specialize\(_2\) uses symbolic addresses and a symbolic store to access and update memory at specialization time. To represent symbolic addresses, we enhance Int32Id in L[IA-32] by adding symbolic constants \((m, n, \ldots)\). A different constant is used to represent the starting address of the stack and each heap block allocated at specialization-time.

\[
\text{Int32Id} = \{\text{EAX, ESP, EBP, ...}, m, n, ...\}
\]

specialize\(_2\) uses a symbolic store \(\text{Store}^{sym}\) instead of \(\text{Store}\).

\[
\rho^{sym} \in \text{Store}^{sym} = \text{RegMap}^{sym} \times \text{FlagMap}^{sym} \times \text{MemMap}^{sym}
\]

\[
\text{RegMap}^{sym} : \text{Int32Id} \rightarrow \text{Term}
\]

\[
\text{FlagMap}^{sym} : \text{BoolId} \rightarrow \text{Formula}
\]

The residual code generated by specialize\(_2\) will use specific run-time addresses to access and update memory using an extra level of indirection. To achieve this effect, specialize\(_2\) uses a memory-layout map \(\mu \in \text{MemLayout}\). A memory-layout map \(\mu\) maps the symbolic starting-address \(m\) of the stack or a heap block to a location \(I\) (register or global address) that holds the run-time counterpart of \(m\).

\[
\mu \in \text{MemLayout} : \text{Int32Id} \rightarrow (\text{Register} \cup \text{INT})
\]

We will illustrate specialize\(_2\), and its constituent functions eval\(_2\) and reduce\(_2\), using the code snippet shown in Fig. 14, which allocates and uses a heap block. (We describe how specialize\(_2\) handles the stack and stack locations at the end of this sub-section.) The snippet has a static call to \(\text{malloc}\) at instruction 2, and static values are written to the allocated heap block at instructions 3 and 4. The binding-time annotations for the instructions are shown as comments on the left-hand column of Fig. 14. Because WiPER lifts all static calls to \(\text{malloc}\), instructions 1 and 2 are lifted.

The algorithms for specialize\(_2\), eval\(_2\), and reduce\(_2\) are given as Algs. 5, 6, and 7, respectively. In Alg. 5, we overload \(\epsilon\) to denote “no symbolic constant” (lines 4 and 13) and “no location” (line 5), respectively. In our example, because instruction 2 allocates memory (checked by Alloc), specialize\(_2\) adds \([m \mapsto \text{EDI}]\) to \(\mu\), where \(m\) is a fresh symbolic constant (obtained using NewConst) that is used to represent the specialization-time starting address of the heap block, and \(\text{EDI}\) is a location that is not used in the residual binary (obtained using NewLoc). This location can also be a global memory location that is otherwise unused in the residual binary. specialize\(_2\) passes \(m\) to eval\(_2\), which stores \(m\) in \(\rho\) under the key NextBlock. eval\(_2\) symbolically executes the instruction using \(\mathcal{I}^{sym}\), which reinterprets the semantics of an instruction I to symbolically execute I. If I allocates memory, \(\mathcal{I}^{sym}\) uses the symbolic constant bound to NextBlock in \(\rho\) as...
the next address in the free list. Consequently, in \( \rho' \) returned by \text{eval} \ for the call to \text{malloc}, \text{EAX} holds the symbolic constant \( m \)—i.e., \( m \) is the starting address of the heap block allocated at instruction 2.

\text{specialize}_2 \ then passes \( I, \rho, \mu, \) and \( EDI \) to \text{reduce}_2. Because instruction 2 allocates memory, \text{reduce}_2 residuates two instructions. The first instruction \((2^R)\) is the call to \text{malloc}; the second instruction \((2^R)\) saves the \text{EAX} register in \( EDI \) (emitted using \text{EmitMove}). After the residual code executes instruction \( 2^R \), the run-time starting address of the heap block will be available in \( EDI \).

\text{specialize}_2 \ symbolically executes the static instruction 3, producing the post-store \( \langle \text{EAX} \mapsto m, [], [m \mapsto 1]\rangle \). While residuating code for lifted instruction 4, \text{reduce}_2 uses \text{Subst}_2 \ to replace all vocabulary-0 terms and formulas in 4’s QFBV formula with terms and formulas, respectively, from the symbolic store. This step produces the formula

\[ \text{Mem}' = \text{Mem} \langle m + 4 \mapsto 2 \rangle. \]

\text{reduce}_2 \ then replaces each symbolic constant \( m \) in the resulting formula with \( [\mu(m)]_L \) using \text{Subst}. For our example, for Eqn. (6), \text{Subst} produces \( \text{Mem}' = \text{Mem} \langle EDI + 4 \mapsto 2 \rangle \). Finally, \text{reduce}_2 \ uses the synthesizer to residuate instruction 4\( _R \) for the specialized formula. One can see that when the residual code executes, instructions 4\( _R \) and 5\( _R \) use the correct starting address of the heap block.

**Handling the stack.** Suppose that \( n \) is the symbolic constant used to denote the specialization-time base of the stack, and \( l \) is a dedicated location that will hold the address of the base of the stack at run-time. Because the stack is typically allocated at the beginning of the program, WiPER adds \([n \mapsto l]\) to \( \mu \) before specialization begins, and emits “\text{mov} l,esp” as the first instruction in the residual program. Additionally, in the initial symbolic store, \( ESP \) is bound to \( n \). In our running example from §3, WiPER adds \([n \mapsto ESP]\) to \( \mu \). Consequently, \text{reduce}_2 \ uses \( ESP \) instead of \( n \) in the QFBV formulas of all downstream lifted instructions.

In summary, to residuate code that is independent of the specialization-time memory layout, \text{specialize}_2 \ uses symbolic addresses, and residuates code that obtains the corresponding run-time addresses from designated locations, using one level of indirection. In effect, the binary is partially evaluated with respect to static values, but not specialization-time addresses.

**PE\(_2\)-Safety.** For \( \text{PE}_2 \) to produce correct residual code for a binary \( B \), \( B \) should be \( \text{PE}_2\)-safe. A binary \( B \), along with a specific division of instructions in \( B \) as static and dynamic, are \( \text{PE}_2\)-safe if they satisfy the following properties:

- **P1** \( B \) does not contain a static branch condition that depends on the starting address of the stack or heap blocks (e.g., \text{cmp esp,1000}).
- **P2** Every static instruction that accesses (updates) memory in block \( M \) only accesses (updates) memory at a static offset from the base of \( M \), and within the bounds of \( M \).

main:

\[
\begin{align*}
A1: \text{mov} & \{\text{esp}\},\text{eax}; S \\
C1: \text{call} & \text{foo} \\
R1: \text{mov} & \{\text{ebp-4}\},\text{eax} \\
\end{align*}
\]

\[
\begin{align*}
&\text{foo:} \\
&: \text{push} \text{ebp} \\
A2: \text{mov} & \{\text{esp}\},\text{eax}; D \\
C2: \text{call} & \text{foo} \\
R2: \text{mov} & \{\text{ebp-8}\},\text{eax} \\
&: \text{pop} \text{ebp} \\
&: \text{ret}
\end{align*}
\]

**Figure 15:** Code snippet to illustrate issues related to interprocedural BTA.

P1 implies that the partial evaluator does not encounter a symbolic branch condition during specialization of \( B \). P2 implies that every term in every store \( \rho^m \) that arises during specialization of \( B \) can be simplified to have the form \( c \), or \( m + c \), where \( c \) is an integer constant, and \( m \) is a symbolic constant.

If a binary \( B \) violates P1 or P2, \( B \) might have different semantics for different layouts of the stack and heap blocks. For example, consider the code snippet

\[
\begin{align*}
1: \text{mov} & \{\text{esp}+1000\}, 10 ; S \\
2: \text{mov} & \{\text{esp} \times 2\}, 20 ; S \\
3: \text{mov} & \text{eax}, \{\text{esp}+1000\}; L
\end{align*}
\]

This snippet violates P2: after symbolically executing instruction 2, we obtain the store \( \rho^m_2 \)

\[
\rho^m_2 \equiv \langle \text{ESP} \mapsto n, [], [n + 1000 \mapsto 10][n \times 2 \mapsto 20]\rangle.
\]

In \( \rho^m_2 \), the term \( n \times 2 \) cannot be rewritten in the form \( m + c \). Note that the value in the \text{EAX} register after (concretely) executing instruction 3 depends on the initial value of \( ESP \). If we execute the snippet with the initial concrete store \( \rho_0 \equiv \langle \text{ESP} \mapsto 1000, [], [], \rangle \), the value in \text{EAX} after executing instruction 3 will be 20. If we execute the code snippet with a different value for \( ESP \) in \( \rho_0 \), the value in \text{EAX} will be 10. Consequently, the snippet loads different values into \text{EAX} for different stack layouts.

Binaries of memory-safe programs produced by a standard compiler are usually \( \text{PE}_2\)-safe. Apart from P1 and P2, we will also require that allocated memory chunks do not overlap in the address space used at run-time. Allocated memory chunks also include the chunk in which the residual code resides. (See §4.4.)

### 4.3 Interprocedural Partial Evaluation

In this section, we present the extensions to the algorithm to handle binaries with multiple procedures.

#### 4.3.1 BTA

For interprocedural partial-evaluation, WiPER uses a monovariant division, i.e., the classification of each instruction as static/dynamic holds for all calling contexts. This approach to BTA introduces the two issues discussed below, which will be illustrated using the code snippet shown in Fig. 15. Procedure \text{main} contains two calls to \text{foo}. The actual parameter of the first call is static, and that of the second call is dynamic. \text{foo} merely returns the formal parameter. (For possible future work on polyvariant BTA, see §8.)
Algorithm 8 specializeFn

Input: CFG, ρ, BTAMap, specializedCFGs
Output: ρ’
1: if (CFG, ρ) ∈ specializedCFGs then
2: return (specializedCFGs[CFG, ρ], specializedCFGs)
3: end if
4: if Recursive(CFG) then
5: specializedCFGs[CFG, ρ] = ρ // See explanation in the text
6: end if
7: (ρ’, specializedCFGs) ← IntraPE(CFG, ρ, BTAMap, specializedCFGs)
8: specializedCFGs[CFG, ρ] = ρ’
9: return (ρ’, specializedCFGs)

Parameter mismatches. A forward slice can include multiple calls to the same procedure, with different subsets of actual parameters at different call-sites. However, the slice contains the union of the corresponding formal-parameter sets, which causes a mismatch between the actual parameters at a call-site and the procedure’s formal parameters [12, 24].

For the moment, assume that the forward slice used by BTA is context-sensitive. In the code snippet shown in Fig. 15, suppose that the slice includes instructions A1 and C1, and the entire body of foo. Note that there is a mismatch between the actual parameter A1, and foo’s formal parameter. (The latter is in the slice, but the former is not.) WIPER lifts instructions A1 and C1 because they are interprocedural predecessors of foo’s instructions; this step ensures that there will be no parameter mismatches in the residual code.

Return mismatches. If the forward slice used during BTA is context-sensitive, there is also a return mismatch between the return value of foo, and the use of the return value at instruction R1. The former is in the slice, but the latter is not, which violates congruence. (At instruction R1, the specialization expects to find a return value for foo in the static store, but there is no value.) To prevent return mismatches, WIPER uses context-insensitive slicing, which causes instruction R1 to be included in the slice.

In summary, for interprocedural BTA, WIPER (i) lifts interprocedural static-predecessors of dynamic instructions, and (ii) uses context-insensitive forward slicing. In addition, to ensure that partial evaluation always terminates, WIPER conservatively classifies all instructions in a recursive procedure as dynamic. (This point is discussed further in §4.3.2.)

4.3.2 Specialization

To perform specialization for interprocedural partial-evaluation, the following lines are added after line [16] of Alg. 3. isCall returns true if the argument is a call instruction; Callee returns the callee CFG for a call instruction.

If isCall(i) then
(ρ, specializedCFGs) ← SpecializeFn(Callee(i), ρ, BTAMap, specializedCFGs)
endif

In addition, Alg. 3 takes an additional argument, specializedCFGs, which is a map whose entries are of the form ⟨CFG, ρ⟩ → ρ’, where ρ is a partial static pre-store and ρ’ is a partial static post-store. Alg. 3 also returns specializedCFGs as an additional return value. Procedure SpecializeFn is given as Alg. 8. Alg. 8 implements function caching—if CFG has already been specialized with respect to ρ, Alg. 8 returns ρ’ (lines 1–3).

To ensure that partial evaluation always terminates, WIPER does not attempt to specialize recursive functions. Recall from §4.3.1 that all instructions in a recursive procedure are classified as dynamic (and the binding-time classification computed by BTA is congruent with respect to that classification). Thus, for a recursive procedure P, the correct values for all variables that are classified static at the return from P are found in the input partial static pre-store ρ. Consequently, Alg. 8 can use ρ as the partial static post-store in the entry added to specializedCFGs before IntraPE is called (lines 4–6). This trick ensures that Alg. 8 cannot get into an infinite loop while specializing a recursive function.

If a function has not already been specialized, Alg. 8 calls Alg. 3 to specialize the CFG with respect to ρ, and adds the partial static post-store to the map (lines 7–8).

4.4 Correctness

In this section, we present two theorems concerning: (i) termination of WIPER, and (ii) correctness of the residual code produced by WIPER. The first theorem applies to binaries with instructions from the entire IA-32 instruction set. Because it would be difficult to prove the correctness theorem for the entire IA-32 ISA, we prove correctness only for binaries containing instructions from a small instruction subset. (See App. A.1.)

Theorem 1. Suppose that B is a PE2-safe binary, and ρsy is a partial static symbolic-store. Then WIPER(B, ρsy) terminates.

Proof. WIPER treats recursive functions conservatively, so WIPER cannot enter into an infinite loop while attempting to specialize a recursive function. WIPER unrolls static loops finitely many times depending upon the static loop bound. Moreover, the forward slice performed during BTA follows both data and control dependences, which rules out the possibility of there being a static instruction that is control dependent on a dynamic branch. Consequently, WIPER cannot create infinitely many specialized versions of the same basic block. Thus WIPER(B, ρsy) is guaranteed to terminate. □

In a standard semantics that formalizes the behavior of an IA-32 processor, an evaluation function would take an IA-32 Store as an input, and produce an IA-32 Store as an output. In §3, we introduced the notion of a state σ consisting of an environment η and an IA-32 store ρ. In this section, we use a non-standard semantics that uses an environment along with an IA-32 store. The environment is really a ghost variable
that makes explicit the starting address of the stack and heap blocks, while the concrete part of the state is the store.

Based on the congruent division established by BTA, a state can be partitioned into $\eta_S$, $\rho_S$, $\eta_D$, and $\rho_D$. Thus the type for the evaluation function $\llbracket\cdot\rrbracket$ (the function that evaluates an instruction or a sequence of instructions with respect to a state, and returns the post-state) can be written as

$$\llbracket\cdot\rrbracket : \text{Instruction} \times \text{Env}_S \times \text{Store}_S \times \text{Env}_D \times \text{Store}_D \rightarrow \text{Env}_S \times \text{Store}_S \times \text{Env}_D \times \text{Store}_D.$$  

If we execute an instruction in a partially evaluated binary, $\rho_S$ is never accessed or updated. Thus we will overload $\llbracket\cdot\rrbracket$ to also denote the meaning function for instructions in a partially evaluated binary:

$$\llbracket\cdot\rrbracket : \text{Instruction} \times \text{Env}_S \times \text{Store}_D \rightarrow \text{Env}_S \times \text{Store}_D$$

It will always be clear from context which meaning of $\llbracket\cdot\rrbracket$ is intended.

We assume that the memory map for a program that has been partially evaluated is equipped with a special area in which the starting addresses of the stack and heap blocks allocated by lifted instructions are stored. Thus, strictly speaking, the memory maps for a binary $B$ and some residual binary $B'$ of $B$ will be different. However, the only differences are in the special area, and we denote equality of two stores $\rho$ and $\bar{\rho}$ modulo the special area by $\rho \approx \bar{\rho}$.

For an input binary $B$ that is $\text{PE}_2$-safe, and an IA-32 state $\sigma$ that can be partitioned into $\eta_S$, $\rho_S$, $\eta_D$, and $\rho_D$ based on a division of inputs to $B$, $\text{WiPER}$ produces a specialized binary that, when executed, produces an answer that matches the answer that would be produced by $B$ (modulo the special area). The precise statement of the property is given in the following theorem:

**Theorem 2.** Suppose that $B$ is $\text{PE}_2$-safe. Also suppose that $\eta_S$ is an environment such that there are no overlaps among (a) any of the chunks in $\text{Dom}(\eta_S)$, (b) the chunk in which the residual code produced by $\text{WiPER}$ is loaded, and (c) any of the chunks allocated during the execution of the residual code. For all $\sigma = (\eta_S, \rho_S, \eta_D, \rho_D)$ such that $[B](\eta_S, \rho_S, \eta_D, \rho_D)$ terminates, suppose that $[B](\eta_S, \rho_S, \eta_D, \rho_D) = (\eta_S', \rho_S', \eta_D', \rho_D')$.

If $\rho_S'$ is a symbolic store such that $\llbracket\cdot\rrbracket_{\rho_S'}(\eta_S) = \rho_S$, then $\llbracket\text{WiPER}(B, \rho_S')\rrbracket_{\eta_S, \eta_D, \rho_D} = (\eta_S', \rho_S', \eta_D', \rho_D')$, where $\rho_D' \approx \rho_D$.

**Proof.** The proof for Thm. 2 is given in App. A.1.

Thm. 2 does not include $\rho_S$ while comparing states because the residual code produced by $\text{WiPER}(B, \rho_S')$ does not contain static instructions, and consequently never accesses or updates the static store $\rho_S$.

**4.5 Threats to Validity**

There are two threats to the validity of our algorithms.

1. If the input binary is not $\text{PE}_2$-safe, the residual code might violate Thm. 2.
2. The accuracy of BTA depends on the accuracy of the SDG for the binary. If the methods used to construct the SDG are overly conservative, BTA can classify instructions as “dynamic” that do not depend on dynamic inputs. If the methods used to construct the SDG are under-approximative, BTA can classify instructions as “static” that actually do depend on dynamic inputs. In our experiments, we observed the former behavior. The SDG that $\text{WiPER}$ uses is built using “variable-like abstractions” recovered by machine-code variable-recovery analyses [9]. Each recovered variable-like abstraction could be imprecise—it is often an agglomeration of some source-code variables. Consequently, the SDG recovered from the program binary could be more imprecise than an SDG that is obtained from the program’s source code. As a result, $\text{WiPER}$’s BTA classifies more instructions dynamic than an analogous BTA that starts from source code.

**5. Implementation**

$\text{WiPER}$ uses CodeSurfer/x86 [10] to obtain the SDG, CFG, and call graph for the binary. $\text{WiPER}$’s BTA uses CodeSurfer/x86’s forward-slicing operation. $\text{WiPER}$’s specializer uses CodeSurfer/x86’s rewriting API to create the sections, CFGs, and instructions in the residual binary. $\text{WiPER}$ uses Transformer Specification Language (TSL) [29] to build its concrete and symbolic interpreters. The concrete operational semantics of the integer subset of IA-32 is written in TSL, and the semantics is interpreted for concrete evaluation, and reinterpreted for symbolic evaluation. $\text{WiPER}$ also uses TSL [30] to convert an instruction into a QFBV formula. $\text{WiPER}$ uses $\text{McSYNTH}$ [45] to synthesize an IA-32 instruction sequence from a QFBV formula. $\text{McSYNTH}$ sometimes requires a set of scratch registers to hold results of intermediate calculations in the residual code. $\text{WiPER}$ supplies dead registers to $\text{McSYNTH}$ to be used as scratch registers. If the number of dead registers at a point is not sufficient, $\text{WiPER}$ supplies global addresses that are unused in the residual program as scratch locations to $\text{McSYNTH}$.

In the examples presented in this paper, we have treated memory as if each memory location holds a 32-bit integer. However, our implementation supports the actual IA-32 memory model, in which each memory location holds an 8-bit integer.

The compiler might add instructions at the beginning of each procedure so that stack variables are aligned on 4-byte, 8-byte, or 16-byte boundaries. For example, consider the code snippet shown in Fig. 16. In procedures $\text{foo}$ and $\text{main}$, the compiler aligns the stack variables on a 16-byte boundary. To accommodate such alignment, we relax P2 of
### Table 1: Characteristics of applications for optimization via specialization.

<table>
<thead>
<tr>
<th>Application</th>
<th>Domain</th>
<th>LOC</th>
<th>Description</th>
<th>Static Input</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mathematical library functions</td>
<td>Linear algebra operations</td>
<td>29</td>
<td>Computes ( z^n )</td>
<td>( n = 100 )</td>
</tr>
<tr>
<td>Interpreter</td>
<td></td>
<td>71</td>
<td>Interpreter for the minimalist language “Brainf*ck”</td>
<td>Input program</td>
</tr>
<tr>
<td>Filter</td>
<td></td>
<td>107</td>
<td>Applies a convolution filter of size ( m \times m ) on an image of size ( n \times n )</td>
<td>( m = 3, n = 3 ), and elements of the filter</td>
</tr>
<tr>
<td>uuencode</td>
<td>Text utilities</td>
<td>129</td>
<td>Base-64 encodes a string of size ( n )</td>
<td>( n = 256 ), and the string</td>
</tr>
<tr>
<td>SHA1</td>
<td>Cryptographic operations</td>
<td>140</td>
<td>Computes the sha1 digest of a message of size ( n ) bits</td>
<td>( n = 1024 ), and contents of the first 512 bits</td>
</tr>
<tr>
<td>uuencode</td>
<td>Text utilities</td>
<td>167</td>
<td>Decodes a base-64-encoded string of size ( n )</td>
<td>( n = 256 ), and the encoded string</td>
</tr>
</tbody>
</table>

```c
foo:
  push ebp
  mov ebp,esp
  and esp,0xFFFF00
  sub esp,170
  ...

main:
  push ebp
  mov ebp,esp
  and esp,0xFFFF00
  sub esp,150
  ...
```

Figure 16: Code snippet to illustrate variable alignment.

PE\(_2\)-safety properties to allow terms of the form \( m + p_0 + p_1 + \ldots + c \), where \( m \) is a symbolic constant representing the specialization-time starting address of the stack or a heap block \( M \), \( c \) is an integer constant, and \( p_0, p_1, \ldots \) are symbolic constants that represent the alignment adjustments performed by the procedures \( Proc0, Proc1, \ldots \) on the current call stack.

If the binary is statically linked, Wi\(_{PER}\) does not need any additional input from the user for partial evaluation. If the binary is not statically linked, the user needs to provide a model for each library function as additional inputs to Wi\(_{PER}\). A model consists of the following information: (i) an input-output dependence relation, and (ii) a procedure to compute return values of library-function calls that are classified as static. Wi\(_{PER}\) specializes library-function calls in a bimodal manner: if any argument to a library-function call is dynamic, all of the static arguments are lifted along with the call; if all arguments are static, Wi\(_{PER}\) uses the user-supplied model to compute a return value for the call (i.e., a fully static call is specialized away.)

We are generally unable to use Wi\(_{PER}\)’s fully automated end-to-end partial-evaluation algorithm to extract components from a large binary. Binaries of large applications do not have clearly demarcated inputs. They often have only one input—a buffer that stores the entire command line. The binary interprets the contents of the buffer to assign values to variables. If the buffer is classified dynamic, Alg. 2 classifies all instructions in the binary dynamic.

For component extraction, we run Wi\(_{PER}\) in an alternative experimental mode, called Component Extraction (CE) mode. In CE-mode, Wi\(_{PER}\) performs a restricted BTA. (The specialization algorithm is the same in CE and non-CE modes.) In CE-mode, the user specifies a subset \( I_5 \) of instructions in the original binary to be treated as static instructions. The remaining instructions in the binary are treated as dynamic instructions. Wi\(_{PER}\) identifies lifted instructions, and then specializes the binary using Wi\(_{PER}\)’s original specialization algorithm.

CE-mode is related to generalized partial computation [22], in which a program is specialized with respect to con-
Compression-decompression utility

Component

<table>
<thead>
<tr>
<th>Application</th>
<th>Size of binary (KB)</th>
<th>No. of procs. in binary</th>
<th>Size of component (KB)</th>
<th>No. of procs. in component</th>
</tr>
</thead>
<tbody>
<tr>
<td>b64</td>
<td>3.4</td>
<td>16</td>
<td>5.9</td>
<td>2</td>
</tr>
<tr>
<td>lzfx</td>
<td>7.6</td>
<td>24</td>
<td>6</td>
<td>8</td>
</tr>
<tr>
<td>bzip2</td>
<td>90.2</td>
<td>117</td>
<td>64.6</td>
<td>78</td>
</tr>
</tbody>
</table>

results are shown in Fig. 17. For these applications, the average speedup produced by partial evaluation, computed via the geometric mean, is 1.3.

For Power, partial evaluation results in a slight slowdown. Power has a tight loop, and we believe that the aggressive loop unrolling caused by partial evaluation disrupts instruction caching.

At the other end of the spectrum, we measured a speedup in Filter of 1.9. Filter has four nested for-loops. The inner two loops iterate over the filter elements. Partial evaluation unrolls all four loops, and—because the filter elements are static—replaces almost all instructions in the bodies of the inner two loops with just a few residual instructions.

6.2 Component Extraction

For this use case, we wanted to answer the following questions:

- How can we extract an executable component from a binary via partial evaluation?
- How does the size of the extracted component compare to the size of the original binary?

For this set of experiments, we used three applications that bundle several components into a bloated executable. Table 2 presents the characteristics of the applications. The first and second applications were obtained from Google Code [1] and SourceForge [2], respectively.

CE-mode of WiPER was used for this set of experiments. The sizes of the original binary and the extracted components are shown in Table 3.

**b64.** The decoder extracted from b64 is bigger than the b64 binary because our current implementation does not optimize the layout of basic blocks in the residual code to reduce the number of jump instructions. For example, b64 has 30 jmp instructions, and the extracted decoder has 164 jmp instructions. The issues in partially evaluating b64 are similar to those of bzip2, which is discussed below.

**lzfx.** Lzfx is a text-compression utility. In this case study, we present how WiPER extracts the compression component of lzfx. The decision about whether to call fx_create (which compresses) or fx_read (which decompresses) is made in the following code snippet from the binary:

```assembly
_loc_80499E2:
_text:08049A84 call fx_read ; D
_text:08049A3A mov eax,dword [esp+44] ;L
_text:08049A3E mov dword [esp+12],eax ;D
_text:080499D4 test eax,eax
_text:080499D6 jnz loc_80499E2
_text:080499D4 call fx_create ; D
_text:080499D4 mov eax,dword [esp+44]
_text:0805B53E cmp eax,1
_text:0805B541 jnz loc_805B558
_text:0805B539 mov eax,[esp+40]
_text:0805B53E cmp eax,1
_text:0805B541 jnz loc_805B558
_text:0805B558 call compress ; D
_text:0805B55B call uncompress ; D
_text:0805B55D: loc_805B55B:
_text:0805B564 call uncompress ; D
```

If the value in the eax register is 0 at instruction 80499D4, lzfx calls fx_create. The user specifies that instructions 80499D4 through 8049A3E should be treated as static instructions. WiPER lifts instruction 8049A3E because it supplies a static value to the dynamic instruction 8049A3E. WiPER performs specialization and evaluates the static and lifted instructions with respect to the partial store

\[ \rho \equiv ([EAX \mapsto 0][ESP \mapsto n], [], []), \]

and residuates the instruction mov eax,0 for the lifted instruction 8049A3E, and emits the remaining dynamic instructions. Because eax is 0 at instruction 80499D4, the fall-through branch is taken at 80499D6, which forces WiPER to enter fx_create and to bypass fx_read. Consequently, WiPER residuates an executable that only performs compression.

With lzfx, we also went further by embedding the extracted compression component in a different application. We created a small header file with the signature of fx_create, and linked the new application with the compression component extracted by WiPER.

**bzip2.** Bzip2 is a large application that takes several auxiliary command-line inputs in addition to one that specifies whether to perform compression or decompression. Ultimately, the decision about whether to call compress or uncompress is made in the following code snippet of the binary:

```assembly
_loc_805B539:
_text:0805B539 mov eax,[esp+40]
_text:0805B53E cmp eax,1
_text:0805B541 jnz loc_805B558
_text:0805B558 call compress ; D
_text:0805B55B call uncompress ; D
_text:0805B55D: loc_805B55B:
_text:0805B564 call uncompress ; D
```

The memory location whose address is ESP + 40 holds a value computed from the compression/decompression flag on the command line. If the value is 1, bzip2 calls compress; otherwise, it calls uncompress.

The user specifies that instructions 805B539 through 805B541 should be treated as static instructions. WiPER specializes and evaluates the aforementioned instructions with respect to the partial store

\[ \rho \equiv ([ESP \mapsto n], [], [n + 40 \mapsto 1]). \]

This partial store forces WiPER to enter compress and bypass uncompress, and consequently WiPER residuates an executable that only performs compression.
7. Related Work

**Partial evaluation.** Partial evaluation has been used as a general framework for the specialization of programs belonging to different languages, and different domains. In addition to several functional languages [25, 32], partial evaluation has been used to specialize a flow-chart language [25], C [6, 15], FORTRAN [26], and Java [40, 41]. Partial evaluators can either be off-line (performed in a single phase) [23], on-line (performed in two phases), or hybrid [41]. WiPER’s high-level architecture resembles that of an off-line partial evaluator for an imperative language. However, the need to handle several machine-code-specific issues makes WiPER’s algorithm significantly different from those of source-code partial evaluators.

**Run-time specialization techniques.** Run-time specialization (or dynamic compilation) generates optimized code during program execution by partially evaluating user-annotated regions of the program with respect to invariant data computed at run time [8, 14, 19, 28].

Like WiPER, these tools perform specialization on machine code. However, the partial-evaluator-like component in such tools is part of the compiler. BTA is performed with respect to source-code variables, and carried out on an IR that is constructed from source code. Run-time-specialization tools have to address an issue that does not arise in WiPER, namely, the need to create code templates that can be reused at run-time. Some tools accomplish this task by jury-rigging an existing compiler’s code generator to inhibit optimizations, such as code motion, by using the volatile type qualifier of C.

In contrast, WiPER faced other issues, such as the need to decouple multiple updates performed by a single instruction, and to create code that allows the stack and heap to be at different positions at run-time than at specialization-time.

**Specialization of Java bytecode.** WiPER is not the first partial evaluator that works on low-level code. Lancet [37] performs partial evaluation of Java bytecode snippets that need to be compiled by a just-in-time (JIT) compiler. JScp [27] performs supercompilation on Java bytecode. Like WiPER, the specializers in Lancet and JScp make use of a static partial store. For Lancet and JScp, the static partial store is a Java virtual-machine (JVM) store, while WiPER’s is an IA-32 store. However, while those specializers work on low-level code, WiPER works at an “even lower level.” The following issues that arise in IA-32 and not in bytecode justify the novel design choices made in WiPER:

1. Because the JVM is a stack-based machine, specialization of bytecode instructions often involves loading constant values instead of locals/fields. In contrast, the operands of IA-32 instructions vary widely, and the specialization of an instruction with respect to a partial store need not be a variant of the instruction. Moreover, IA-32 has around 43,000 unique opcodes, and WiPER’s specializer must be able to specialize any instruction with respect to any partial store. WiPER addressed this issue by using machine-code synthesis.

2. Address computation is not explicit in bytecode (variables are referenced using offsets). Consequently, bytecode specialization does not face the problem of residuating specialization-time addresses. However in machine code, instructions compute addresses, and a naïve specializer, such as PE, is unsatisfactory. For this reason, WiPER uses symbolic techniques for specialization.

**Superoptimization and link-time optimization.** Superoptimization aims at finding an optimal instruction-sequence for a target instruction-sequence [11, 31, 39]. Peephole superoptimization [11] uses “peepholes” to harvest target instruction-sequences, and replace them with equivalent instruction-sequences that have a lower cost. Link-time optimizers carry out whole-program optimizations at link time [33]. While these optimization techniques optimize a binary for all possible inputs, WiPER optimizes a binary for a specific input.

8. Conclusion and Future Work

In this paper, we presented an algorithm for machine-code partial evaluation. We presented WiPER, a partial evaluator for IA-32. We used WiPER to partially evaluate the binaries of seven test applications with respect to static inputs, and obtained specialized binaries that had an average speedup of 1.3 (computed via the geometric mean). We also presented two case studies that describe how WiPER can be used to extract an executable component from a bloated binary.

One possible direction for future work is to investigate polyvariant BTA via specialization slicing [7]. For every call to a procedure P with a different combination of static and dynamic actual parameters, specialization slicing can be used to produce a different binding-time annotation for P’s instructions. This technique could increase the number of static instructions during specialization, leading to residual code that is more specialized than the code currently residuated by WiPER. A second direction is to use liveness information to reduce the number of specialized copies of a basic block produced by WiPER.

**Acknowledgments**

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**References**

A. Appendix

Theorem 2. Suppose that $B$ is $PE_{\Sigma}$-safe. Also suppose that $\eta_S$ is an environment such that there are no overlaps among (a) any of the chunks in $\text{Dom}(\eta_S)$, (b) the chunk in which the residual code produced by $\text{WiPER}$ is loaded, and (c) any of the chunks allocated during the execution of the residual code. For all $\sigma = (\eta_S, \rho_S, \eta_D, \rho_D)$ such that $B(\eta_S, \rho_S, \eta_D, \rho_D)$ terminates, suppose that $B(\eta_S, \rho_S, \eta_D, \rho_D) = (\eta_S, \eta_D, \rho_D)$. If $\rho_S^{sym}$ is a symbolic store such that $[\rho_S^{sym}] (\eta_S) = \rho_S$, then $[\text{WiPER}(B, \rho_S^{sym})] (\eta_S, \eta_D, \rho_D) = (\eta_S, \eta_D, \rho_D)$, where $\rho_D \approx \rho_D'$. 

A.1 Proof of Thm. 2

We prove Thm. 2 for binaries whose instructions come from a small subset of the IA-32 instruction set, TinyIA32. TinyIA32 consists of a small subset of the IA-32 instruction set, augmented with (i) an extra register, and (ii) two new instructions. We decided to exclude instructions related to branches and function calls from TinyIA32 because if we were to prove Thm. 2 for the entire IA-32 ISA, the part of the proof concerning branches and function calls would be similar to that of an analogous proof for a source-code partial evaluator. We prove Thm. 2 using induction on the length of the trace of a run of the binary, and it is straightforward to extend our trace-based proof to an ISA that includes branches and function calls.

TinyIA32 has three registers, no flags, and seven instructions. The abstract syntax of TinyIA32 is defined in Fig. 18. In an indirect operand, the register holds the address of the memory location. For instructions with two operands, the operand on the left is the destination operand. For the heapalloc instruction, the single operand is the destination operand. For the stackalloc instruction, the single operand is both a source and destination operand.
We assume the following: 

- \( \text{INT} := \{ \ldots, -1, 0, 1, \ldots \} \)
- \( \text{Reg} := r_1 \mid r_2 \mid rw_1 \)
- \( R := \text{Direct} (\text{Reg}) \)
- \( C := \text{Imm} (\text{INT}) \)
- \( M := \text{Indirect} (R) \)
- \( I := \text{mov} (R, C) \mid \text{mov} (R_1, R_2) \mid \text{mov} (R, M) \mid \text{mov} (M, R) \)
- \( \text{add} (R_1, R_2) \mid \text{stackalloc} (R) \mid \text{heapalloc} (R) \)

Figure 18: Abstract syntax of TinyIA32.

The register \( rw_1 \) is a work register that is used for holding the results of intermediate calculations in residual code. A work register is used to simulate the fact that the real \( \text{WIPER} \) uses dead registers as scratch registers for such calculations. In the rest of this section, we do not show the work register in TinyIA32 stores. Also, if a register is not used in a TinyIA32 binary, it has the default value 0.

The first \( \text{mov} \) instruction loads a 32-bit constant into a register. The second \( \text{mov} \) instruction performs a register-to-register move. The final two \( \text{mov} \) instructions move a 32-bit value from a memory location to a register and from a register to a memory location, respectively. The \( \text{add} \) instruction adds the 32-bit values in the two register operands, leaving the result in the destination operand register. The \( \text{stackalloc} (R) \) instruction allocates a stack of some fixed, but arbitrarily large, size, whose starting address is available as an output in \( R \). The \( \text{heapalloc} (R) \) instruction allocates a heap block whose size is provided as an input in \( R \), and whose starting address is returned in \( R \) as the output. Because TinyIA32 has no flags, a TinyIA32 store consists of only a register map and a memory map.

We prove Thm. 2 by induction on the length \( n \) of a partial trace \( T \) of a run of binary \( B \).

**A.1.1 Base Case** \( n = 0 \)

Thm. 2 trivially holds on a partial trace with no instructions.

**A.1.2 Induction Hypothesis**

Let us assume that Thm. 2 holds on a partial trace \( T \equiv I_1, I_2, \ldots, I_n \) with \( n \) instructions. Suppose that the corresponding residual trace produced by \( \text{WIPER} \) for \( T \) is \( T' \equiv J_1, J_2, \ldots, J_n \), where \( J_i \) is the residual instruction sequence produced by the \( \text{Specialize} \) phase of \( \text{WIPER} \) for \( I_i \). (Note that \( J_i \) can be an empty sequence of instructions or can consist of several instructions.) Suppose that the initial state is \( (\eta_S, \rho_S, \eta_D, \rho_D) \). (Recall from §3 that \( \eta \) maps a symbolic constant denoting the starting address of the stack or a heap block to a concrete address.) As the induction hypothesis, we assume the following:

\[
\begin{align*}
[I_1, I_2, \ldots, I_n] (\eta_S, \rho_S, \eta_D, \rho_D) &= (\eta^n_S, \rho^n_S, \eta^n_D, \rho^n_D) \\
\land [J_1, J_2, \ldots, J_n] (\eta_S, \eta_D, \rho_D) &= (\eta^n_S, \eta^n_D, \rho^n_D) \\
\land \eta^n_D &\approx \rho^n_D
\end{align*}
\]

To account for the actions of \( \text{WIPER} \) on static and lifted instructions, we need to introduce yet one more ghost variable, \( \text{ghostStaticStore} (\text{gSS}) \). At each point \( k \) in the trace \( T' \), this variable holds the static symbolic store that was used by \( \text{WIPER} \) to create the next residual instruction-sequence in \( T' \), i.e., \( J_{k+1} = \text{Specialize} (I_{k+1}, \text{gSS}^k) \).

We strengthen the induction hypothesis with the following conjunct:

\[
[\text{gSS}^n] \theta^n_S = \rho^n_S,
\]

where the left-hand side denotes the simplification of each symbolic expression in \( \text{gSS} \) with respect to the values obtained from \( \eta^n_S \). Because \( \text{gSS}^0 \) is \( \rho^n_S \), by the hypothesis \( \rho^n_S \approx (\eta^n_S, \rho^n_S, \eta^n_D, \rho^n_D) \) in Thm. 2, we have \( [\text{gSS}^0] (\eta_S) = \rho_S \), and thus Eqn. (8) holds for the base case.

**A.1.3 Induction Step**

We now prove Thm. 2 on a partial trace \( I_1, I_2, \ldots, I_{n+1} \) with \( n + 1 \) instructions. That is, the goal is to show

\[
[I_1, I_2, \ldots, I_{n+1}] (\eta_S, \rho_S, \eta_D, \rho_D) = (\eta^n_S, \rho^n_S, \eta^n_D, \rho^n_D)
\]

\[
\land [J_1, J_2, \ldots, J_{n+1}] (\eta_S, \eta_D, \rho_D) = (\eta^n_S, \eta^n_D, \rho^n_D)
\]

\[
\land \eta^n_D \approx \rho^n_D
\]

\[
\land [\text{gSS}^n] \theta^n_S = \rho^n_S.
\]

Some additional intuition about the induction hypothesis can be obtained from the following more precise restatement of reparenthesization (5):

\[
l : (\eta_S, \rho_S, \eta_D, \rho_D) \rightarrow (l, \text{gSS}) : (\eta_S, \eta_D, \rho_D)
\]

where \( \rho_S = [\text{gSS}] \theta_S \).

There are three subcases, for \( I_{n+1} \) being static, lifted, or dynamic.

**A.1.3.1 Static instructions.** Because static-allocation sites are lifted—see line [10] of Alg. 2—a static instruction cannot have the form \( \text{stackalloc} (R) \) or \( \text{heapalloc} (R) \). The argument for each of the static-instruction cases for \( I_{n+1} \) has the following form: Suppose that instruction \( I_{n+1} \) is static. Then

\[
[I_{n+1}] (\eta^n_S, \rho^n_S, \eta^n_D, \rho^n_D) = (\eta^n_S, \rho^n_S, \eta^n_D, \rho^n_D)
\]

\[
\land \text{where some update is made to } \rho^n_S \text{ to create } \rho^{n+1}_S
\]

\[
\text{Specialize}(I_{n+1}, \text{gSS}^n) \equiv J_{n+1} = \epsilon
\]

where \( \epsilon \) denotes the empty sequence of instructions. Because \( J_{n+1} \) is empty, we have

\[
[I_{n+1}] (\eta^n_S, \eta^n_D, \rho^n_D) = (\eta^n_S, \eta^n_D, \rho^n_D)
\]

Eqns. (11) and (12), together with Eqn. (7), show that Eqn. (9) holds.

The congruence property of BTA ensures that \( \text{WIPER} \) can completely evaluate \( I_{n+1} \) at specialization time, and \( \text{gSS}^n \) is updated by \( \text{WIPER} \) to produce \( \text{gSS}^{n+1} \) in the same way as \( \rho^n_S \) is updated by \( I_{n+1} \) to produce \( \rho^{n+1}_S \). Moreover, because \( \eta^n_S \) is not updated by \( I_{n+1} \), by Eqn. (8) we have \( [\text{gSS}^{n+1}] \theta^n_S = \rho^{n+1}_S \), and Eqn. (10) holds. Consequently, the induction hypothesis holds on a trace with \( n + 1 \) instructions, where the \( (n + 1)^{th} \) instruction is static.
A.1.3.2 Lifted and dynamic instructions. We now make an observation that is relied on in many of the cases—namely, because static-allocation sites are lifted, if instruction \( I_1 \) in \( T \) is an allocation instruction, then \( J_1 \) in \( T' \) also contains an allocation instruction, i.e., the allocations in the two traces are in lock-step. For purposes of the proof, we can assume that \( B \) and \( \text{WiPER}(B, \rho_S^\text{sym}) \) are run in environments that will perform storage allocation in the same way. Consequently, if \( I_1 \) allocates the stack or a heap block \( M \) at address \( m \), an instruction in \( J_1 \) also allocates \( M \) at \( m \). In the respective semantics, such allocations will be recorded by updating \( \eta \) to \( \eta[m \mapsto m] \), where \( m \) is a symbolic constant that denotes the starting address of \( M \). (Lifted allocation instructions update \( \eta_S \) and \( \eta_D \); dynamic allocation instructions update \( \eta_{D'} \).)

Dynamic instructions. The argument for each of the dynamic-instruction cases for \( I_{n+1} \), except stackalloc and heapalloc, has the following form: Suppose that instruction \( I_{n+1} \) is dynamic. Then

\[
[I_{n+1}]([\eta^m_S, \rho^m_S, \eta^m_D, \rho^m_D]) = ([\eta^m_S, \rho^m_S, \eta^m_D, \rho^m_D]),
\]

where some update is made to \( \rho^m_D \) to create \( \rho^{m+1}_D \).

\[
\text{Specialize}(I_{n+1}, gSS^n) \equiv J_{n+1} = I_{n+1}
\]

Because \( J_{n+1} \) is the same as \( I_{n+1} \), we have

\[
[I_{n+1}]([\eta^n_D, \rho^n_D, \eta^n_D, \rho^n_D]) = ([\eta^n_D, \rho^n_D, \eta^n_D, \rho^{n+1}_D]),
\]

where \( \rho^{n+1}_D \) is \( \rho^{n+1}_D \). Eqsns. (13) and (14), together with Eqn. (7), show that Eqn. (10) holds.

The static components of the state, \( \eta_S^n \), \( gSS^n \), and \( \rho^S_n \) are left unchanged, so Eqn. (10) holds.

The cases for stackalloc and heapalloc are similar, except that those instructions update \( \eta^n_D \) in addition to \( \rho^n_D \). Moreover, because of our assumption about the storage allocator, the updates to \( \eta^n_D \) by \( [I_{n+1}] \) and \( [J_{n+1}] \) are identical, and the updates to \( \rho^n_D \) by \( [I_{n+1}] \) and \( [J_{n+1}] \) are also identical. Consequently, the induction hypothesis holds on a trace with \( n + 1 \) instructions, where the \( (n + 1)^{st} \) instruction is dynamic.

Lifted instructions. The semantics we use for evaluating static and dynamic instructions is fairly standard—static instructions access and update \( \rho_S \), and dynamic instructions access and update \( \rho_D \) (in addition to updating \( \eta_D \)). However, the evaluation of lifted instructions is non-standard: lifted instructions were originally classified static, so they must be evaluated just like static instructions; however, they also take "snapshots" of the current static state and dump them into \( \eta_D \) and \( \rho_D \) for use by downstream dynamic instructions.

Lifted instructions access \( \rho_S \), but produce values that might be consumed by dynamic successors, so they must update \( \rho_D \). In addition, lifted instructions can also have static successors, so they must also update \( \rho_S \). Thus, in the semantics used for the original program, a lifted instruction performs the same update on both \( \rho_S \) and \( \rho_D \). In the semantics used for the residual program, it updates only \( \rho_D \) because \( \rho_S \) is not present in states. However, for the purposes of this proof, an appropriate update is performed on \( gSS \).

Similarly, if a lifted instruction allocates memory, both static and dynamic instructions downstream might access or update locations in the allocated memory. Thus in both semantics, if a lifted instruction allocates memory, it performs identical updates on \( \eta_S \) and \( \eta_D \).

The non-overlap hypothesis of Thm. 2, together with property P2 of \( \text{PE}_2 \)-safety, imply that each specialization-time address can be represented canonically by a term of the form \( m + c \), where \( m \) is the symbolic constant that denotes the starting address of the stack or a heap block \( M \), and \( c \) is a constant offset.

The actual symbolic constants used are essentially arbitrary (as long as each new symbolic constant is fresh). However, for the purposes of the proof, we need to relate the symbolic constants used by the original program to those in the residual program. Thus, for the purposes of the proof, we assume that when \( \text{WiPER} \) partially evaluates a lifted instruction \( I_1 \) in \( T \) that allocates memory, the symbolic constant \( m \) that should be used in \( gSS \) to denote the starting address of the allocated stack or heap block is supplied by an oracle. This oracle ensures that the same symbolic constant \( m \) gets added to the ghost variables \( \eta_S \) and \( \eta_D \) when \( I_1 \) and the allocation instruction in \( J_1 \) are evaluated. (If the oracle did not ensure this concordance, we cannot establish the equality in Eqn. (8).) \( \text{WiPER} \) binds \( m \) to a dedicated global address \( M-\text{addr} \), and uses \( M-\text{addr} \) in the residual code to save the concrete starting address \( m \) of the allocated memory. \( (M-\text{addr} \) is located in the special area in the memory map of the residual program discussed in §4.4. Recall from §4.2.2.3 that \( \text{WiPER} \) uses a memory-layout map \( \mu \) to bind a symbolic constant to a dedicated location.)

We handle the lifted-instruction cases according to the form of the instruction. In the cases below, we abbreviate an update to the register map as \( \rho[R] \mapsto v \) rather than let \( (rm, mm) = \rho \in (rm[R] \mapsto v), \) and similarly use \( \rho[a \mapsto v] \), to denote an update to the memory map at address a. Which kind of map-update operation is intended should be clear from context.

1. \( I_{n+1} = \text{mov}(\text{Direct}(R), \text{Imm}(v)):\)

\[
[I_{n+1}]([\eta^n_S, \rho^n_S, \eta^n_D, \rho^n_D]) = ([\eta^n_S, \rho^n_S, \eta^n_D, \rho^n_D][R \mapsto v])
\]

\[
\text{Specialize}(I_{n+1}, gSS^n) \equiv J_{n+1} = \text{mov} \, r1, v
\]

\[
[I_{n+1}]([\eta^n_S, \rho^n_S, \eta^n_D, \rho^n_D]) = ([\eta^n_S, \rho^n_S, \eta^n_D, \rho^n_D][R \mapsto v])
\]

Eqns. (15), (16), and (7) show that Eqn. (9) holds.

\[
gSS^{n+1} = gSS^n[R \mapsto v]
\]

\[
\eta_S^{n+1} = \eta_S^n \text{ and } \rho_S^{n+1} = \rho_S^n[R \mapsto v] \text{ (From (15))}
\]

Eqns. (17), (18), and (8) show that Eqn. (10) holds.
2. $I_{n+1} = \text{mov}(\text{Direct}(R1), \text{Direct}(R2))$: There are two cases that can arise.

(a) Suppose that $\rho_S(R2) = u$ and $gSS^u(R2) = v$.

$$[I_{n+1}](\eta^+_S, \rho_S, \eta^-_D, \rho^-_D) = (\eta^+_S, \rho^+_S[R1 \mapsto u], \eta^-_D, \rho^-_D[R1 \mapsto u])$$ (19)

simplify([I_{n+1}](gSS^u)) ≜ $J_{n+1} = \text{mov \ r1, v}$

$$[J_{n+1}](\eta^+_S, \eta^-_D, \rho_D) = (\eta^+_S, \eta^-_D, \rho_D[R1 \mapsto v])$$ (20)

$u = \rho^+_S(R2) = ([gSS^u]n)^S(R2)$ (By Eqn. (8))

$$= ([gSS^u(R2)]\eta^+_S) = [v]n\eta^+_S = v$$ (21)

Eqns. (19)–(21), and (7) show that Eqn. (9) holds.

$$gSS^{n+1} = gSS^u[R1 \mapsto v]$$ (22)

$$\eta^+_{S}^{n+1} = \eta^+_S$$ and $\rho^+_{S}^{n+1} = \rho^+_S[R1 \mapsto u]$ (From (19)) (23)

Eqns. (21)–(23), and (8) show that Eqn. (10) holds.

(b) Suppose that $\rho^+_{S}(R2) = u$ and $gSS^u(R2) = m + c$.

simplify([I_{n+1}](gSS^u)) ≜ $J_{n+1} = \text{mov \ r1, M-addr}$

$$\text{mov} \ r1, [rwl]; \text{mov} \ rwl, c; \text{add} \ r1, rw1; \text{mov} \ rw1, 0$$

$$[J_{n+1}](\eta^+_S, \eta^-_D, \rho_D) = (\eta^+_S, \eta^-_D, \rho_D[R1 \mapsto m+c])$$ (24)

$u = \rho^+_S(R2) = ([gSS^u]n)^S(R2)$ (By Eqn. (8))

$$= ([gSS^u(R2)]\eta^+_S) = [m + c]\eta^+_S = m + c$$ (25)

Eqns. (19), (24), (25), and (7) show that Eqn. (9) holds.

$$\eta^+_{S}^{n+1} = \eta^+_S$$ and $\rho^+_{S}^{n+1} = \rho^+_S[R1 \mapsto u]$ (From (19)) (27)

Eqns. (25)–(27), and (8) show that Eqn. (10) holds. Note that $J_{n+1}$ has the mov $rwl, 0$ instruction at the end of the residual code to restore the default value 0 in work register $rwl$.

3. $I_{n+1} = \text{mov}(\text{Direct}(R1), \text{Indirect}(R2))$: Because $R2$ must hold an address, there are two cases that can arise.

(a) Suppose that $\rho^+_S(R2) = a$ and $\rho^+_S(a) = u$, and $gSS^u(R2) = m + c$ and $gSS^a(m + c) = v$.

$$[I_{n+1}](\eta^+_S, \rho^+_S, \eta^-_D, \rho^-_D) = (\eta^+_S, \rho^+_S[R1 \mapsto u], \eta^-_D, \rho^-_D[R1 \mapsto u])$$ (28)

simplify([I_{n+1}](gSS^u)) ≜ $J_{n+1} = \text{mov \ r1, v}$

$$[J_{n+1}](\eta^+_S, \eta^-_D, \rho_D) = (\eta^+_S, \eta^-_D, \rho_D[R1 \mapsto v])$$ (29)

$u = \rho^+_S(a) = \rho^+_S(\rho^+_S(R2))$

$$= \rho^+_S(([[gSS^u]]n)^S(R2)) = [m + c]\eta^+_S$$ (By Eqn. (8))

$$= ([gSS^u(R2)]\eta^+_S) = [m + c]\eta^+_S = v$$ (30)

Eqns. (28)–(30), and (7) show that Eqn. (9) holds.

$$gSS^{n+1} = gSS^u[R1 \mapsto v]$$ (31)

$$\eta^+_{S}^{n+1} = \eta^+_S$$ and $\rho^+_{S}^{n+1} = \rho^+_S[R1 \mapsto u]$ (From (28)) (32)

Eqns. (30)–(32), and (8) show that Eqn. (10) holds.

(b) Suppose that $\rho^+_S(R2) = a$ and $\rho^+_S(a) = u$, and $gSS^a(R2) = m + c$ and $gSS^u(m + c) = m + c$.

simplify([I_{n+1}](gSS^a)) ≜ $J_{n+1} = \text{mov \ r1, M-addr}$

$$\text{mov} \ r1, [rwl]; \text{mov} \ rwl, c; \text{add} \ r1, rw1; \text{mov} \ rw1, 0$$

$$[J_{n+1}](\eta^+_S, \eta^-_D, \rho_D) = (\eta^+_S, \eta^-_D, \rho_D[R1 \mapsto m+c])$$ (33)

$u = \rho^+_S(a) = \rho^+_S(\rho^+_S(R2))$

$$= \rho^+_S(([[gSS^u]]n)^S(R2)) = [m + c]\eta^+_S$$ (By Eqn. (8))

$$= ([gSS^u(R2)]\eta^+_S) = [m + c]\eta^+_S = m + c$$ (34)

Eqns. (28), (33), (34), and (7) show that Eqn. (9) holds.

$$gSS^{n+1} = gSS^a[R1 \mapsto m+c]$$ (35)

$$\eta^+_{S}^{n+1} = \eta^+_S$$ and $\rho^+_{S}^{n+1} = \rho^+_S[R1 \mapsto u]$ (From (28)) (36)

Eqns. (34)–(36), and (8) show that Eqn. (10) holds.

4. $I_{n+1} = \text{mov}(\text{Indirect}(R1), \text{Direct}(R2))$: Because $R1$ must hold an address, there are two cases that can arise.

(a) Suppose that $\rho^+_S(R1) = a$ and $\rho^+_S(a) = u$, and $gSS^a(R1) = m + c$ and $gSS^u(R2) = v$.

$$[I_{n+1}](\eta^+_S, \rho^+_S, \eta^-_D, \rho^-_D) = (\eta^+_S, \rho^+_S[R1 \mapsto u], \eta^-_D, \rho^-_D[R1 \mapsto u])$$ (37)

simplify([I_{n+1}](gSS^u)) ≜ $J_{n+1} = \text{mov \ r1, v}$

$$[J_{n+1}](\eta^+_S, \eta^-_D, \rho_D) = (\eta^+_S, \eta^-_D, \rho_D[R1 \mapsto v])$$ (38)

Similar to the proof of Eqn. (21), we can prove that $u = v$. Similar to the proof of Eqn. (25), we can prove that $a = m + c$. These equalities, together with Eqns. (37), (38), and (7), show that Eqn. (9) holds.

$$gSS^{n+1} = gSS^u[m + c \mapsto v]$$ (39)

$$\eta^+_{S}^{n+1} = \eta^+_S$$ and $\rho^+_{S}^{n+1} = \rho^+_S[a \mapsto u]$ (From (37)) (40)

The equalities $u = v$ and $a = m + c$, along with Eqns. (39), (40), and Eqn. (8), show that Eqn. (10) holds.
(b) Suppose that $\rho_S^a(R1) = a$ and $\rho_S^b(R2) = u$, and $gSS^n(R1) = m_1 + c_1$ and $gSS^n(R2) = m_2 + c_2$.

$\text{Specialize}(I_{n+1}, gSS^n) \equiv J_{n+1} = \text{mov} \; rwl_1, M-addr$;
$\quad \text{mov} \; rwl_1, [rwl_1]; \text{mov} \; rwl_1, c_1; \text{add} \; r1, rwl_1;
\quad \text{mov} \; rwl_1, M-addr; \text{mov} \; r2, [rwl_1];
\quad \text{mov} \; rwl, c_2; \text{add} \; r2, rwl; \text{mov} \; [r1], r2;
\quad \text{mov} \; rwl, 0 \quad [J_{n+1}](\eta_S^n, \eta_D^n, \eta_D^n) = (\eta_S^n, \eta_D^n, \eta_D^n[m_1+c_1 \rightarrow m_2+c_2])$ (41)

Similar to the proof of Eqn. (25), we can prove that $a = m_1 + c_1$ and $u = m_2 + c_2$. These equalities, together with Eqns. (37), (41), and (7), show that Eqn. (9) holds.

\begin{align*}
gSS^{n+1} &= gSS^n[m_1 + c_1 \rightarrow m_2 + c_2] \quad (42) \\
\eta_S^{n+1} &= \eta_S^n \quad \text{and} \quad \rho_S^{n+1} = \rho_S^n[a \rightarrow u] \quad \text{(By Eqn. (37))} (43)
\end{align*}

The equalities $a = m_1 + c_1$ and $u = m_2 + c_2$, along with Eqns. (42), (43), and (8), show that Eqn. (10) holds.

5. $I_{n+1} = \text{add}(\text{Direct}(R1), \text{Direct}(R2))$ There are two cases that can arise.

(a) Suppose that $\rho_S^a(R1) + \rho_S^b(R2) = u$, and $gSS^n(R1) + gSS^n(R2) = v$.

\begin{align*}
\quad [J_{n+1}](\eta_S^n, \rho_S^n, \eta_D^n, \rho_D^n) =
\quad (\eta_S^n, \rho_S^n[R1 \rightarrow m], \eta_D^n, \rho_D^n[R1 \rightarrow m]) \quad (44)
\end{align*}

$\text{specialize}(I_{n+1}, gSS^n) \equiv J_{n+1} = \text{mov} \; r1, v$

\begin{align*}
\quad [J_{n+1}](\eta_S^n, \eta_D^n, \rho_D^n) &= (\eta_S^n, \eta_D^n, \rho_D^n[R1 \rightarrow m]) \quad (45)
\end{align*}

$\quad u = \rho_S^n(R1) + \rho_S^n(R2) = 
\quad = (gSS^n[R1] \rightarrow (gSS^n[R2]) \quad (\text{By Eqn. (8)}) \\
\quad = (gSS^n(R1)) \eta_S^n + (gSS^n(R2)) \eta_S^n \\
\quad = (gSS^n(R1) + gSS^n(R2)) \eta_S^n \quad [v] \eta_S^n = v \quad (46)
\end{align*}

Eqns. (44)–(46), and (7) show that Eqn. (9) holds.

\begin{align*}
\quad gSS^{n+1} &= gSS^n[R1 \rightarrow v] \quad (47)
\quad \eta_S^{n+1} &= \eta_S^n \quad \text{and} \quad \rho_S^{n+1} = \rho_S^n[R1 \rightarrow m] \quad \text{(From (44))} \quad (48)
\end{align*}

Eqns. (46)–(48), and (8) show that Eqn. (10) holds.

(b) Suppose that $\rho_S^a(R1) + \rho_S^b(R2) = u$, and $gSS^n(R1) + gSS^n(R2) = m + c$.

\begin{align*}
\text{specialize}(I_{n+1}, gSS^n) \equiv J_{n+1} = \text{mov} \; rwl, M-addr$;
\quad \text{mov} \; r1, [rwl]; \text{mov} \; rwl, c; \text{add} \; r1, rwl;
\quad \text{mov} \; rwl, 0 \quad [J_{n+1}](\eta_S^n, \eta_D^n, \rho_D^n) = (\eta_S^n, \eta_D^n, \rho_D^n[R1 \rightarrow m + c]) \quad (49)
\end{align*}

\begin{align*}
\quad u &= \rho_S^n(R1) + \rho_S^n(R2) = 
\quad = (gSS^n[R1]) + (gSS^n[R2]) \quad (\text{By Eqn. (8)}) \\
\quad &= (gSS^n(R1)) \eta_S^n + (gSS^n(R2)) \eta_S^n \\
\quad &= (gSS^n(R1) + gSS^n(R2)) \eta_S^n \\
\quad &= [m + c] \eta_S^n = m + c \quad (50)
\end{align*}

Eqns. (44), (49), (50), and (7) show that Eqn. (9) holds.

\begin{align*}
\quad gSS^{n+1} &= gSS^n[R1 \rightarrow m + c] \quad (51)
\quad \eta_S^{n+1} &= \eta_S^n \quad \text{and} \quad \rho_S^{n+1} = \rho_S^n[R1 \rightarrow m] \quad (\text{From (44)}) \quad (52)
\end{align*}

Eqns. (50)–(52), and (8) show that Eqn. (10) holds.

6. $I_{n+1} = \text{stackalloc}(\text{Direct}(R1))$

\begin{align*}
\quad [I_{n+1}](\eta_S^n, \rho_S^n, \eta_D^n, \rho_D^n) = (\eta_S^n[m \rightarrow m], \rho_S^n[R1 \rightarrow m], \eta_D^n[m \rightarrow m], \rho_D^n[R1 \rightarrow m]) \quad (53)
\end{align*}

$\text{Specialize}(I_{n+1}, gSS^n) \equiv J_{n+1} = \text{mov} \; r1, m-addr$;
\quad \text{mov} \; rwl, m-addr; \text{mov} \; [rwl], r1; \text{mov} \; rwl, 0 \quad [J_{n+1}](\eta_S^n, \eta_D^n, \rho_D^n) = (\eta_S^n[m \rightarrow m], \eta_D^n[m \rightarrow m], \rho_D^n[R1 \rightarrow m] \quad (54)
\end{align*}

\begin{align*}
\quad \eta_D^n = \eta_D^n \quad \text{and} \quad \rho_D^n = \rho_D^n[R1 \rightarrow m] \quad \text{(By Eqn. (53))} \quad (56)
\end{align*}

Note that the oracle supplies the correct $m$ while updating $gSS$, and WiPER uses $m$ to obtain the correct $m$-addr to use in the residual code. Eqns. (55), (56), and (8) show that Eqn. (10) holds.

7. $I_{n+1} = \text{heapalloc}(\text{Direct}(R1))$

\begin{align*}
\quad [I_{n+1}](\eta_S^n, \rho_S^n, \eta_D^n, \rho_D^n) = (\eta_S^n[m \rightarrow m], \rho_S^n[R1 \rightarrow m], \eta_D^n[m \rightarrow m], \rho_D^n[R1 \rightarrow m]) \quad (57)
\end{align*}

$\text{Specialize}(I_{n+1}, gSS^n) \equiv J_{n+1} = \text{heapalloc} r1$;
\quad \text{mov} \; rwl, M-addr; \text{mov} \; [rwl], r1; \text{mov} \; rwl, 0 \quad [J_{n+1}](\eta_S^n, \eta_D^n, \rho_D^n) = (\eta_S^n[m \rightarrow m], \eta_D^n[m \rightarrow m], \rho_D^n[R1 \rightarrow m] \quad (58)
$p_{D}^{n+1} \approx \rho_{D}^{n+1}$ because $M$-addr is in the special area of the memory map of the residual binary. This observation, along with Eqns. (57), (58), and (7), show that Eqn. (9) holds.

\begin{align*}
gSS^{n+1} &= gSS^{n}[RI \mapsto m] \quad (59) \\
\eta_{S}^{n+1} &= \eta_{S}^{n}[m \mapsto m] \text{ and } \rho_{S}^{n+1} = \rho_{S}^{n}[RI \mapsto m] \\
(By \text{ Eqn. (57))} \quad (60)
\end{align*}

Note that the oracle supplies the correct $m$ while updating $gSS$, and WiPER uses $m$ to obtain the correct $M$-addr to use in the residual code. Eqns. (59), (60), and (8) show that Eqn. (10) holds. \qed