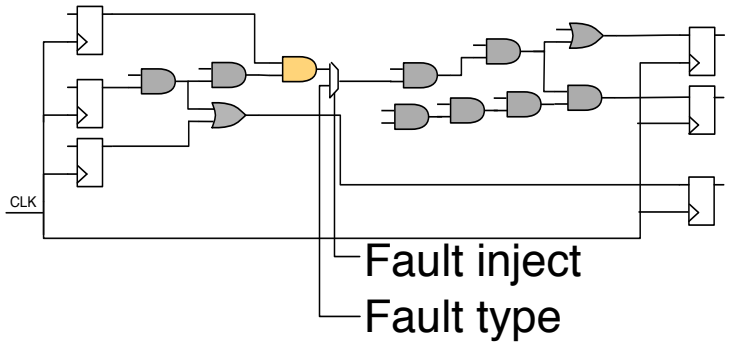
OpenRISC RTL +
new reliability technique



Add fault injection logic

Architectural state
(PC, Register writes…)

OpenRISC
RTL + fault
injection logic

RAM

Add logic to log
architecture state

Xilinx ISE

Fault
Vector

B

Propagation delay,
circuit level logic faults

Zynq
FPGA

C

Arch
Error Trace