Crossing Guard: Mediating Host-Accelerator Coherence Interactions

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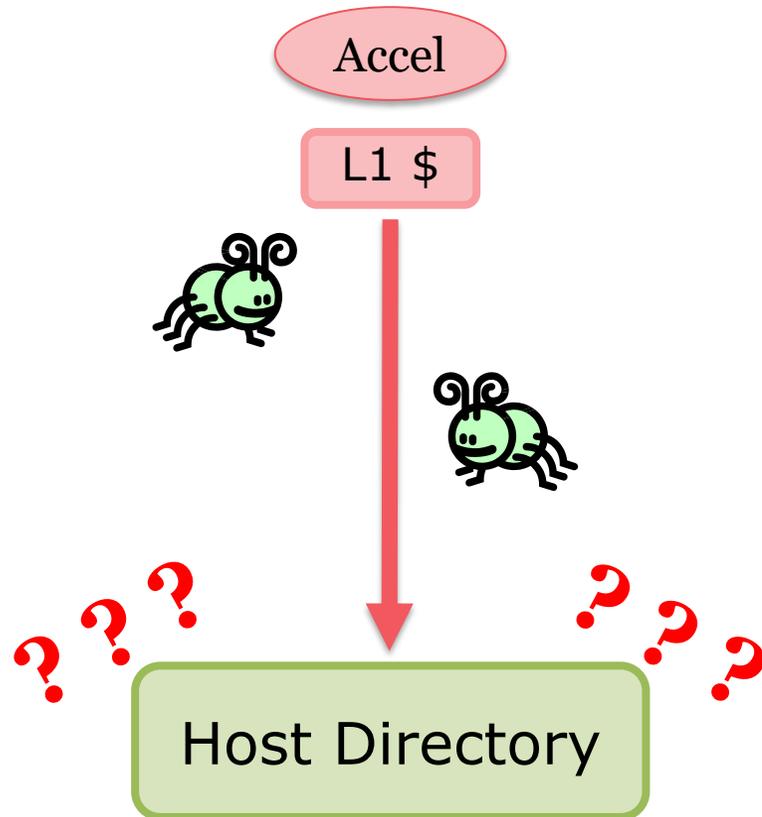
- Complex, programmable accelerators increasingly prevalent

- Many applications: graphics, scientific computing, video encoding, machine learning, etc...

- Accelerators may benefit from cache coherent shared memory
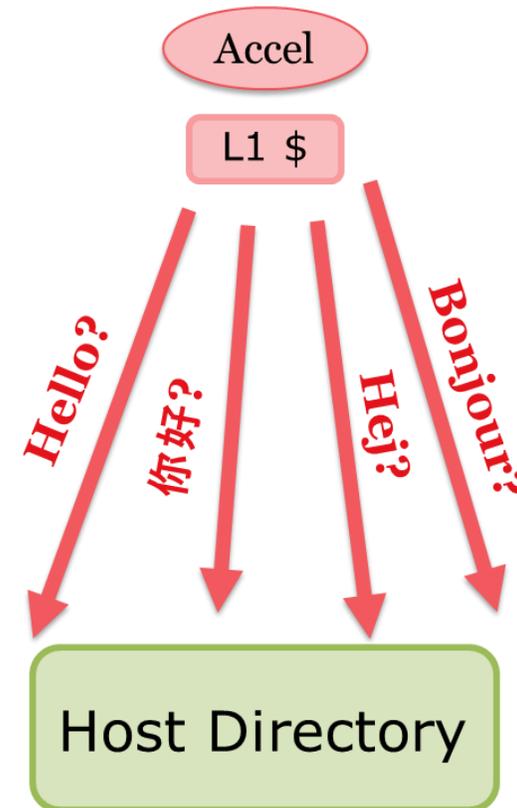
- May be designed by third parties

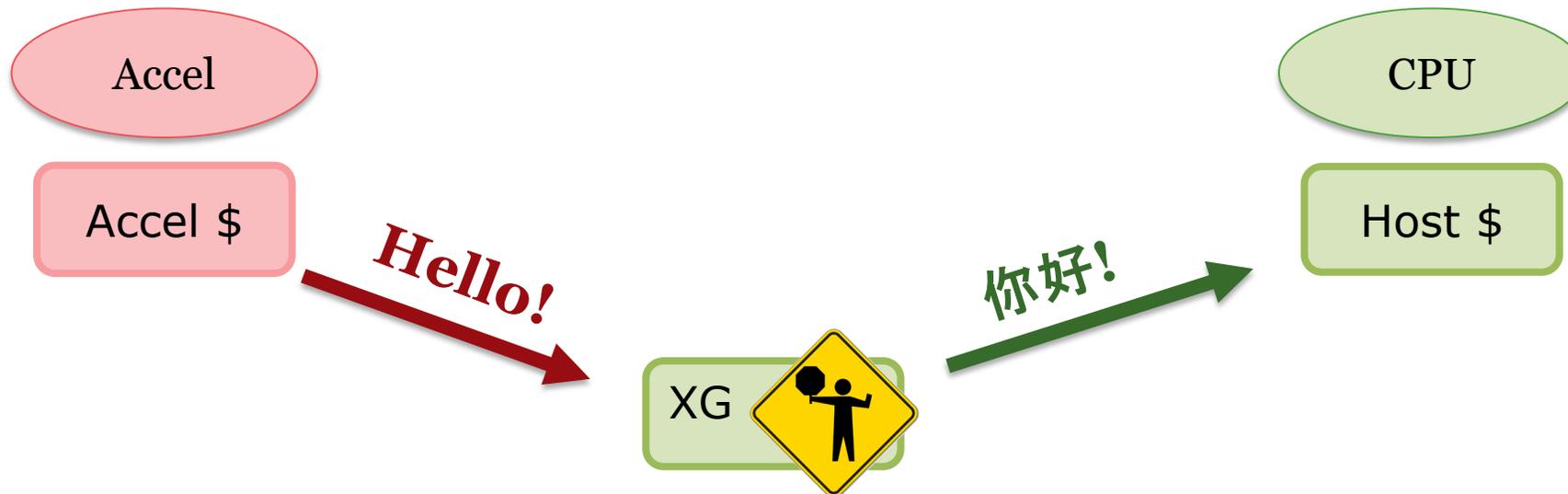# However...

Accelerator coherence bugs can crash host system!

Different host systems use different coherence protocols!

Crossing Guard

Crossing Guard: coherence interface to safely translate accelerator ↔ host protocol

L1 Controller without Crossing Guard…

	Ifetch	Load	Store	Invalidate	Other GETS only	Other GETS	Merged GETS	Other GETX	Ack	Shared Ack	Data	Shared Data	Exclusive Data	Writeback Ack	Writeback Nack	All acks	All acks no sharers	L2 Replacement	L1 to L2	Trigger L2 to L1D	Trigger L2 to L1I	Complete L2 to L1
I	j i a u im u m k / IS	i i a u dm u m k / IS	i i b u dm u m k / IM	f l	f l	f l		f l														
S	h u ih k	h u dh k	i b u dm u m k / SM	f cc g r l / I	f l	f l		f cc g r l / I											cc r ka / I	i g v li s	i r i fu s z ll / ST	i r j fu s z ll / ST	
O	h u ih k	h u dh k	i b u dm u m k / OM	e cc g r l / I	e l	e l	em l	e cc g r l / I											i d cc r ka / OI	i g v li s	i r i fu s z ll / OT	i r j fu s z ll / OT	
M	h u ih k	h u dh k	h u dh k / MM	c cc g r l / I	e l / O	e l / O	em l / O	c cc g r l / I											i d cc r ka / MI	i g v li s	i r i fu s z ll / MT	i r j fu s z ll / MT	
MM	h u ih k	h u dh k	h u dh k	c cc g r l / I	e l / O	c cc g r l / I	em l / O	c cc g r l / I											i d cc r ka / MI	i g v li s	i r i fu s z ll / MMT	i r j fu s z ll / MMT	
IR	j i a u im u m k / IS	i i a u dm u m k / IS	i i b u dm u m k / IM	z																	z	
SR	h u im u h k ka / S	h u dm u h k ka / S	i b u dm u m k / SM	z	z	z		z													z	
OR	h u im u h k ka / O	h u dm u h k ka / O	i b u dm u m k / OM	z	z	z		z													z	
MR	h u im u h k ka / M	h u dm u h k ka / M	h u dm u h k ka / MM	z	z	z		z													z	
MMR	h u im u h k ka / MM	h u dm u h k ka / MM	h u dm u h k ka / MM	z	z	z		z													z	
IM	z	z	z	f l	f l	f l		f l	m o n		u m o n / ISM		u m o sx n kd / MM^W				kk gm sxt s j kd / MM	z		z		
SM	h u ih k	h u dh k	z	f cc l / IM	f l	f l		f cc l / IM	m o n		v m o n / ISM		v m o n / ISM				kk sxt gm s j kd / MM	z		z		
OM	h u ih k	h u dh k	z	e cc l / IM	e l	e l	em l	e cc l / IM	m o n		kk m o n		kk m o n			sxt gm s j kd / MM	sxt gm s j kd / MM	z		z		
ISM	h u ih k	h u dh k	z						m o n		kk m o n		kk m o n				sxt gm s j kd / MM	z		z		
M^W	h u ih k	h u dh k	h u dh k / MM^W						m o n	kk m o n	kk m o n	kk m o n	kk m o n			kk gm s j kd / M	gm s j kd / M	z		z		
MM^W	h u ih k	h u dh k	h u dh k						m o n	kk m o n	kk m o n	kk m o n	kk m o n			kk gm s j kd / MM	gm s j kd / MM	z		z		
IS	z	z	z	f l	f l	f l		f l	m o n	m r o n	u m o hx uo n kd / SS	u r m o hx uo n kd / SS	u m o hx n kd / M^W			kk gs s h j kd / O	kk gs s h j kd / O	z		z		
SS	h u ih k	h u dh k	z						m o n	m r o n	kk m o n	kk m o n	kk m o n			gs s j kd / S	gs s j kd / S	z		z		
OI	z	z	z	q l / II	sq l	sq l	qm l	q l / II						q s l kd / I	kk s l kd / I			z		z		
MI	z	z	z	q l / II	sq l / OI	sq l / OI	qm l / OI	q l / II						t s l kd / I	kk s l kd / I			z		z		
II	z	z	z	f l	f l	f l		f l						g s l kd / I	s l kd / I			z		z		
ST	z	z	z	z	z	z	z	z										z		z		j kd / SR
OT	z	z	z	z	z	z	z	z										z		z		j kd / OR
MT	z	z	z	z	z	z	z	z										z		z		j kd / MR
MMT	z	z	z	z	z	z	z	z										z		z		j kd / MMR

L1 Controller with Crossing Guard

	Load	Store	Replacement	Invalidate	DataM	DataE	DataS	Writeback Ack
M	h q	hh q	j v cm l / B	d l m / I				
E	h q	hh q / M	j v ce l / B	dc l m / I				
S	h q	s j b / B	cs j v l / B	f l m / I				
I	i j a / B	i j b / B		f m				
B	zz	zz		f m	u k n / M	w u k n / E	w u k n / S	k n / I